How to Use ICeGaN™

Overview

This document describes the main features of Cambridge GaN Devices' (CGD) Integrated Circuit Enhancement-mode Gallium Nitride (ICeGaN) HEMT and outlines the key considerations a design engineer should take when implementing a CGD ICeGaN transistor in their design. The document will explain the key differences between ICeGaN and discrete GaN transistors, and how to make use of these differences to create simpler, more efficient and high-power density power converters.

This document is aimed at design engineers with switch mode power supply (SMPS) design experience, and assumes the reader is familiar with the use of MOSFETs or IGBTs in power conversion applications.

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Nomenclature

V_{DS}, v_{DS}	Drain to Source Voltage	
V_{GS}, v_{GS}	Gate to Source Voltage	
V_{DD}	ICeGaN Supply Voltage	
V_{CC}	Gate Driver Supply Voltage	
$V_{GS(th)}$	Gate to Source Threshold	
V_{SD}	Source to Drain Voltage	
$V_{GS(high)}$	Gate to Source Voltage when Gate Driver is High	
$R_{DS(on)}$	Drain to Source On Resistance	
I_G	Gate to Source Current	
I_{VDD}	V_{DD} Current	
BV_{DS}	Drain to Source Blocking Voltage	
C_{OSS}	Output Capacitance	
C_{ISS}	Input Capacitance	
C_{RSS}	Reverse Transfer Capacitance	
Q_{OSS}	Output Charge	
Q_{RR}	Reverse Recovery Charge	
Q_G	Gate Charge	
E_{OSS}	C_{OSS} Stored Energy	
R_{G-on}	Turn-on Gate Resistor	
R_{G-off}	Turn-off Gate Resistor	
T	Temperature	
t_{d-on}	Turn-on Delay Time	
t_{d-off}	Turn-off Delay Time	
t_{rise}	V_{DS} Rise Time	
t_{fall}	V_{DS} Fall Time	

1 Introduction to ICeGaN™ Technology

ICeGaN stands for "Integrated Circuit Enhancement-mode GaN". It is a technology based on an enhancement mode GaN HEMT (e-mode GaN or e-GaN) aimed at lowering losses and running more efficiently than silicon super-junction (SJ) MOSFET and silicon carbide (SiC) MOSFET solutions. For a given on-state resistance, e-mode GaN devices have extremely low parasitic capacitances, C_{ISS}, C_{OSS}, and C_{RSS}. This, combined with the zero reverse recovery loss of e-mode GaN devices, allows engineers to optimise their SMPS designs further than would be possible with MOSFETs, enabling more efficient, more power dense designs. This is particularly important for topologies typically operated in a hard-commutation condition, such as CCM Totem Pole Boost PFC, Multi-level Flying Capacitor, and Dual Active Bridge.

The p-GaN gate structure is used in the majority of e-mode GaN technologies in the semiconductor market. One drawback of e-mode GaN devices is that they have a relatively low threshold voltage (1.2 V for ohmic p-GaN gate and 1.7 V for the more widely adopted Schottky p-GaN gate [1]) and a low maximum gate-to-source voltage of typically ~6 V. These two gate characteristics can be problematic when using e-mode GaN devices in the noisy environment of switched mode power supplies. Consequently, designers of SMPS must put extra effort when designing driving circuits for discrete e-mode GaN devices [2]. The typical solution utilises both a clamping circuit to limit the positive driving voltage level, and a negative 'gate-low' driving voltage to avoid any potential parasitic turn-on during fast dv/dt or di/dt in the transition time. This approach increases the driving circuit design complexity, and lessens the SMPS reliability. It further has secondary detrimental effects such as worsening EMI, increasing third quadrant losses, and some literature has suggested it can even impact dynamic R_{ON} performance [2] [3]. A co-pack approach, where the gate driver circuit is fully integrated in the e-mode GaN package, can simplify the PCB layout design, however, the heat generated by the power device can cause heating in the driver, compromising its performance. This is particularly an issue in higher power, low $R_{DS(on)}$, GaN HEMTs where the required gate charge from the driver is larger.

To address these issues, ICeGaN has been designed to improve gate reliability while maintaining the driver external to the device. ICeGaN has a higher threshold voltage of 2.9 V, while being capable of being driven with gate voltages of up to 20 V, significantly higher than that of other discrete e-mode GaN devices [4]. Furthermore, the turn-on slew rate of ICeGaN can be controlled by the turn-on driving resistor value, meaning designers can control the turn-on switching speed of ICeGaN according to the application specific needs, and balance between EMI and switching losses. In addition, the ICeGaN H2 series has an NL[3] (No Load and Light Load) circuit (patent pending) to ensure efficient no-load and light-load operation.
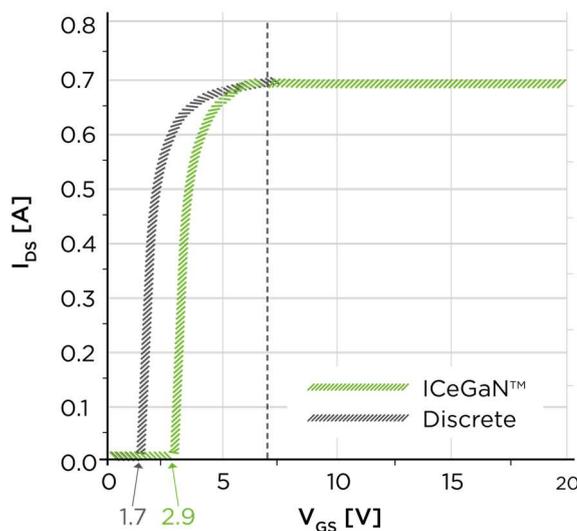

Figure 1 - ICeGaN transfer characteristics with higher $V_{GS(th)}$ and extended maximum gate voltage vs discrete GaN.

2 What is ICeGaN™

This chapter will begin discussing why it is advantageous for an SMPS designer to utilise e-mode GaN in their designs. It will go on to discuss the internal structure of ICeGaN, and how the individual parts of the IC enhance the performance of the e-GaN HEMT. Finally, the benefits of ICeGaN for a design engineer will be highlighted.

2.1 GaN HEMT and ICeGaN Advantages

See below two tables comparing the key device parameters and performance metrics of ICeGaN with discrete e-GaN, SiC MOSFET and two silicon Super-junction (SJ) MOSFETs.

Part Number	Device Type	BV_{DS} [V]	$R_{DS(on)}$ (typ) [mΩ]	Continuous V_{GS} [V]	$V_{GS(th)}$ (typ) [V]
IPX65R065C7 [5]	SJ Si MOSFET	650	58	-20 to +20	3.5
IPP65R060CFD7 [6]	SJ Si MOSFET (FBD)[1]	650	52	-20 to +20	4
IMZ65R057M1H [7]	SiC MOSFET	650	57	-2 to +20	4.5
GS66508X [8]	Discrete e-GaN	650	50	-10 to +7	1.7
CGD65A055S2 [9]	ICeGaN	650	55	0 to +20	2.9
CGD65A055SH2 [10]	ICeGaN	650	55	0 to +20	2.9

Table 1 – Comparison of key device parameters of SJ SiMOS, SiCMOS, discrete e-mode GaN, and ICeGaN.

Part Number	Device Type	$R_{DS(on)}$ x Q_{OSS}* [mΩ x μC]	$R_{DS(on)}$ x Q_{RR} [mΩ x μC]	$R_{DS(on)}$ x E_{OSS}* [mΩ x μJ]	$R_{DS(on)}$ x Q_G [mΩ x nC]
IPX65R065C7	Si SJ MOSFET	12.88	580	552	3712
IPP65R060CFD7	Si SJ MOSFET (FBD)	Not Specified	44.72	494	3536
IMZ65R057M1H	SiC MOSFET	3.71	6.44	559	1596
GS66508X	Discrete e-GaN	3.20	0	400	305
CGD65A055S2	ICeGaN	3.47	0	440	330
CGD65A055SH2	ICeGaN	2.59	0	319	220

Table 2 - Comparison of key performance metrics of SJ SiMOS, SiCMOS, discrete e-mode GaN, and ICeGaN.

*Evaluated at 400 V.

GaN HEMTs offer improved switching performance [2] over SJ silicon MOSFETs and SiC MOSFETs as shown in Table 1 and Table 2. The zero reverse recovery loss ($R_{DS(on)}$ x Q_{RR}) and low hard-switching losses ($R_{DS(on)}$ x E_{OSS}) give significant benefits in hard-commutation, half-bridge based topologies such as totem-pole boost converter. The low output charge ($R_{DS(on)}$ x Q_{OSS}) and low gate driving loss are key to increasing the switching frequency in resonant zero-voltage-switching (ZVS) topologies such as LLC. The order of magnitude lower gate charge, Q_G, makes driving easier, gate driving less lossy, and reduces switching times. GaN HEMTs offer the best performance for all these switching parameters compared to SJ Si MOSFETs and SiC MOSFETs. Although not included in the table, it is worth noting that GaN HEMTs, much like SJ Si MOSFETs, have a monotonic positive temperature coefficient of the channel resistance, which allows for easy parallel operation with good current sharing. Conversely, SiC MOSFETs do not always have a monotonic behaviour for $R_{DS(on)}$ vs temperature. This can add complexity to ensuring good current sharing when SiC MOSFETs are paralleled.

The upcoming Open Compute Project specification for datacentre modular hardware system-common redundant power supplies is expected to require ~50 W/inch³ power density with 97.5% half load efficiency, and 96.5% full load efficiency at 5.5 kW. As power density and efficiency requirements continue to become more challenging, power supply designers will be forced to utilise GaN HEMTs to increase the power supply switching frequency and fulfil these high power density and

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[1] IPX65R065CFD7 is a SJ MOSFET with 'fast body diode' (FBD). It is optimised to minimise Q_{RR}.

high efficiency requirements. Cambridge GaN Devices offers such devices with the superior performance that will be essential in the near future, together with integrated smart features that dramatically simplify GaN integration into a solution when compared to other discrete e-GaN.

2.2 Internal Architecture of ICeGaN

Figure 2 shows a simplified internal functional block diagram of ICeGaN. ICeGaN is an e-mode GaN HEMT with integrated on-chip features such as: Miller Clamp for reliable turn-off, Auxiliary HEMT for an increased threshold voltage and wide range of turn-on gate driving voltages, NL^3 circuit for reducing no-load power consumption (H2 series only), and ESD protection. ICeGaN H1 and H2 series devices have 6 pins. Four of the pins are like that of a standard, discrete 4-pin power device: Gate, Kelvin Source (KS), Drain, and Source pins. The extra two pins are VDD and Current Sense (CS). The VDD pin must be supplied with a voltage source (9 V to 20 V) to power the internal circuitry of ICeGaN. The CS pin provides a current output that is a fixed proportion of the drain current. This signal can be used within the control loop for current mode control or could alternatively be used for over current protection (OCP).
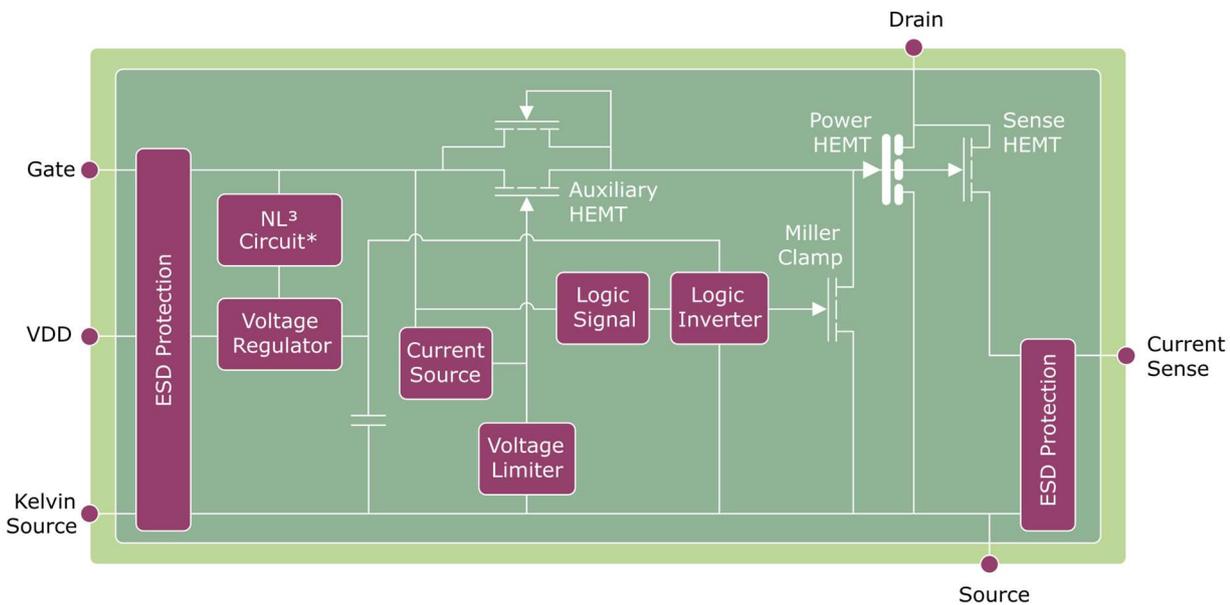

Figure 2 - Simplified internal functional blocks of ICeGaN.

NL^3 curcuit is only present in H2 ICeGaN.

2.2.1 Gate Characteristics and the Auxiliary HEMT

Key to the improved transfer characteristic is the Auxiliary HEMT. It is this transistor that allows for the external gate to exceed the 6 V typically specified by discrete e-mode GaN. The current source provides a constant current to the voltage limiter, which clamps the gate of the auxiliary HEMT approximately a threshold above the desired gate voltage of the Power HEMT. The voltage relationship of Gate pin to the 'internal' gate of the Power HEMT is shown in Figure 3 at 25 °C.

It can be seen that the internal gate of the Power HEMT only begins to increase once the external gate has exceeded approximately 1.5 V. It is this additional threshold that allows ICeGaN to have a higher threshold voltage than conventional discrete e-mode GaN at 2.9 V. Once the internal Power HEMT gate voltage reaches 4.7 V it begins to become clamped. The clamping is achieved through a combination of the Current Source and Voltage Limiter setting the gate voltage of the Auxilary HEMT as seen in the block diagram in Figure 2. This limits the current consumption in this clamping condition and keeps the gate driving losses at an acceptable level.
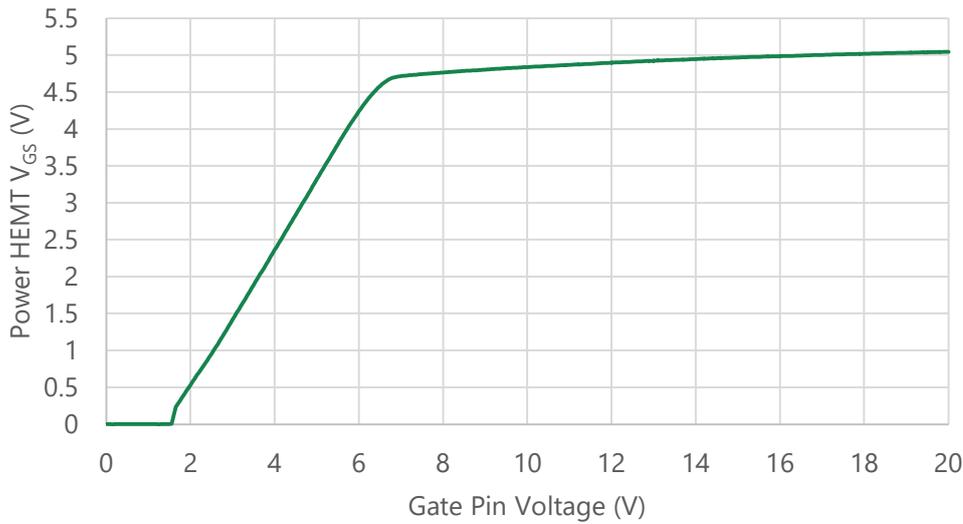
Figure 3 - Relationship between gate voltage and power HEMT gate voltage within ICeGaN at 25ºC.

Having control over the gate voltage of the Power HEMT allows for additional improvements to the performance of the GaN HEMT. It has been well documented in academic literature that it is desirable to drive Schottky e-GaN HEMTs with larger gate voltages at higher temperatures [11] [12]. ICeGaN incorporates a temperature dependence on the Voltage Limiter, allowing the Power HEMT to be driven on with higher gate voltages at higher temperatures. This will improve the long-term reliability of the GaN HEMT.

Further, the ICeGaN interface dramatically improves the transient withstand capability of the gate [13]. It has been shown that the transient capability of the gate for a 20 ns pulse is vastly improved over discrete e-GaN, increasing from 27.5 V to 79 V in hard switching 150 ºC. ICeGaN has been shown to have transient performance superior to the tested SiC MOSFET (C3M0120065D) and comparable performance to the tested Si IGBT (RGT8NS65D). The tabulated results from this paper are included below [13].

Switching Condition	Si IGBT	SiC MOSFET	Discrete p-GaN HEMT	ICeGaN
SSW, 25ºC	78 V	64 V	23 V	66 V
SSW, 150ºC	78 V	64 V	25 V	72 V
HSW, 25ºC	78 V	64 V	25.5 V	72 V
HSW, 150ºC	78 V	64 V	27 V	79 V

Table 3 - Dynamic gate breakdown voltage for four devices at gate overshoot pulse width 20 ns.

2.2.2 Miller Clamp

CGD includes a monolithically integrated Miller Clamp on the GaN die that is scaled in size depending on the $R_{DS(on)}$ of the Power HEMT. This is dual purpose. First, it ensures the device is held in an off state while there is no gate voltage present. Because it is monolithic, it offers the path of lowest possible inductance to the Power HEMT's source, and consequently provides optimal dv/dt protection to prevent spurious turn-on. Secondly, it provides an extremely fast path to discharge the gate capacitance and turn the device off when the external gate pin is pulled low.

2.2.3 NL³ Circuit and H2 No Load Consumption

Unique to ICeGaN H2 series is the NL³ circuit. This is an adaptive power consumption circuit that reduces the power consumption of VDD when the gate is low. Having a low power mode such as this is essential if the SMPS is to meet the

increasingly stringent regulatory requirements for no load and light load conditions, particularly for consumer power adapters. The NL[3] circuit deactivates specific blocks within the ICeGaN, leaving only those essential to keep the device in a safe off state, such as the Miller Clamp. When the gate is pulled high, the NL[3] block immediately reenables these deactivated blocks such that the turn-on performance is unaffected.

2.2.4 Current Sense HEMT

The current sense HEMT outputs a proportional fraction of the main drain current through the current sense pin. Physically, the current sense HEMT is a small fraction of the larger Power HEMT, and shares a common drain, and a common gate, but with a separate source. This means that the two devices switch simultaneously, but the smaller Current Sense HEMT outputs a proportionally smaller current through its source, the current sense pin. This allows the design engineer to observe the device current without having to disrupt the main power loop, which would introduce additional resistive loss for shunt resistors, or stray inductance with current sense transformers. Further, a measurement of the device current can be taken while the device source, the main cooling path, is still soldered directly onto the ground plane, allowing for more optimal device cooling.
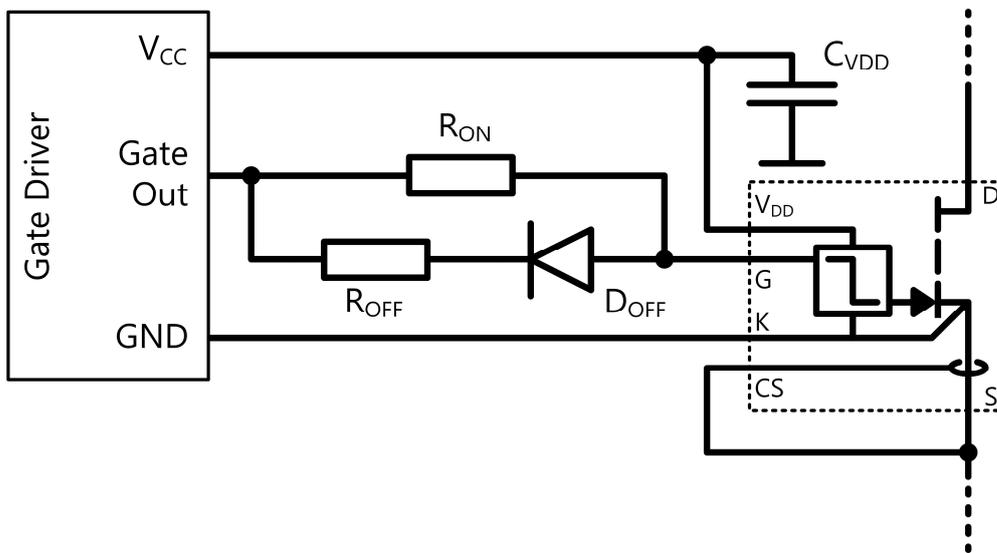
2.3 Ease of Use

Figure 4 - Schematic example of connecting ICeGaN to a gate driver.

Unlike discrete e-mode GaN, ICeGaN is directly compatible with traditional MOSFET gate driver ICs. Figure 4 shows the connection between ICeGaN and a MOSFET gate driver IC with a single output gate driver. Only 4 passive components are required for driving ICeGaN: R_{ON}, R_{OFF}, D_{OFF}, and C_{VDD}. Since the V_{DD} voltage range of ICeGaN is from 9 V to 20 V, the gate driver IC supply voltage can be directly used for the ICeGaN supply voltage V_{DD}, with the filter capacitor C_{VDD} recommended to be fitted locally to the ICeGaN device. Typically, CGD suggests this capacitor is small, at approximately 100 nF. R_{ON}, together with gate voltage when high ($V_{GS(high)}$), determines the driving current to charge the Power HEMT input capacitance of ICeGaN. Consequently, these two variables will control the turn-on switching speed (assuming the source current capability of the driver is not reached). During turn-off, most of the gate charge is dissipated through the internal Miller Clamp, meaning switching speed is largely independent of R_{OFF}. R_{OFF} will however impact turn-off delay, and therefore it is recommended that R_{OFF} should be small to reduce this delay as much as possible. CGD recommends a value for R_{OFF} < 10 Ω, typically 2.2 Ω. Consequently, the separate turn-off path, with R_{OFF} and D_{OFF}, is only required when R_{ON} has been made

large by the design engineer, likely to slow switching slew rate for EMI/EMC purposes. If a driver with separate turn-on and turn-off paths is implemented, then there is of course no need for D_{OFF} and R_{OFF} would be recommended to be small.

With discrete e-GaN, negative gate voltages, while not strictly required for the off-state gate voltage to be below threshold, are typically used to prevent spurious turn-on events triggered by coupling into the gate from dv/dt events on the drain [2]. ICeGaN does not have this concern, and consequently never requires negative gate voltages. This is due to the combination of the Auxiliary HEMT and the integrated Miller Clamp. The Auxiliary HEMT increases the external threshold of the ICeGaN such that the voltage on the gate pin is practically doubled before a turn-on could occur. Simultaneously, the Miller Clamp provides an ultra-low impedance path from the internal gate directly to device Kelvin. While solutions using discrete e-GaN could match the low resistance of the Miller Clamp to their gate driver pull down, they can never be as effective at preventing spurious turn-on since the Miller Clamp is monolithically integrated on the die. This integration provides a route with extremely low stray inductance. While increasing device reliability, these features also allow the gate loop design to be less critical and accordingly lessen the burden on the PCB design engineer to optimise this routing.

3   Using ICeGaN™

This chapter will initially discuss the ICeGaN datasheet, with a focus on the parameters that are different to those of discrete e-GaN devices. Following this, the switching behaviour of ICeGaN will be discussed, including how to control the drain to source slew rate of the device. Finally, the practical implementation of the device in the SMPS will be discussed along with an alternative means of powering the VDD pin.

3.1   Key Parameters in an ICeGaN Datasheet

Compared to discrete e-mode GaN HEMT device parameters, ICeGaN has some additional parameters provided in the datasheet, and others that are affected by the ICeGaN interface. In this section, a detailed explanation will be given for these parameters including $V_{GS(th)}$, V_{GS}, V_{DD}, V_{SD}, and CS.

3.1.1   Voltage on the Gate

As has been discussed in chapter 1 and shown in Figure 1, ICeGaN has an improved transfer characteristics when compared to discrete Schottky gate e-mode GaN HEMTs. The threshold voltage of ICeGaN is 2.9 V (typical value). The auxiliary HEMT restrains the maximum V_{GS} of the Power HEMT to around 5 V at 25 °C, allowing the maximum continuous external gate voltage for ICeGaN to be 20 V.

The peak voltage of the Gate pin must be lower than the V_{DD} value in static conditions. Under abnormal switching operations, such as the power converter at start up, transient load, no load, and short circuit, the maximum allowable transient voltage of the Gate is 1.5 V plus V_{DD} and the maximum transient negative Gate voltage is -1.5 V.

3.1.2   Gate Current Consumption and Gate Charge

ICeGaN uses the current provided to the Gate to directly charge the Power HEMT gate. For this reason, the device has a Q_G comparable to that of discrete e-GaN. This means that during the turn-on transition, the device will consume as much peak current as the driver, and driving circuit, can supply. Once the Power HEMT has been fully enhanced, the consumed gate current will drop to ~3 mA. The exact consumption will depend on the part number utilised. For specifics the datasheet should be consulted. This current is used to bias the voltage regulator and keep the device in its optimal operational condition. When the device is turned off, most of the Power HEMT's gate charge will be discharged through the internal Miller Clamp. For this reason, externally measured $Q_{G(on)} \neq Q_{G(off)}$.

3.1.3 V_{DD} Supply Range and Current Consumption

The VDD pin supply range mimics that of the Gate pin, being 9 V to 20 V, with the additional condition that $V_{DD} > V_G$ at all times. It is expected that the supply voltage for ICeGaN V_{DD} and the gate driver V_{CC} will be common, and so meeting this requirement will not usually be an issue.

VDD pin current consumption is quoted in the ICeGaN H2 series datasheet in the following way. The specific example is the 55 mΩ CGD65A055SH2.

Parameter		Conditions	Min	Typ	Max	Unit
V_{DD} Current (V_{GS} in on-state)	I_{VDD}	V_{GS} = 12 V, V_{DS} = 0 V		1	1.6	mA
V_{DD} Current (V_{GS} in on-state)	I_{VDD}	T_J = 150 °C, V_{GS} = 12 V, V_{DS} = 0 V		0.5		mA
V_{DD} Current (V_{GS} in off-state)	I_{VDD}	V_{GS} = 0 V, V_{DS} = 0 V		70	150	µA
V_{DD} Current (V_{GS} in off-state)	I_{VDD}	T_J = 150 °C, V_{GS} = 0 V, V_{DS} = 0 V		35		µA
V_{DD} Start-up Current	I_{VDD_start}	V_{GS} = 0 V, V_{DS} = 0 V		250		µA

Table 4 - VDD current consumption of CGD65A055SH2.

While the gate is high, ICeGaN consumes ~ 1 mA though the VDD pin. When the gate is low, the V_{DD} current is very small at 70 µA at 25 °C. In this condition the Miller clamp is actively driven on, and the device is safe against dv/dt induced false turn-on events. The low VDD pin consumption is a consequence of the integrated NL[3] circuit that allows ICeGaN to provide excellent no load and light load performance. During start-up the VDD pin must be supplied with 250 µA to ensure the pin can be brought up. Once V_{DD} is established (V_{DD} > 9 V), the current consumption will drop to the steady state value, I_{VDD}.

3.1.4 Reverse Conduction and V_{SD}

Unlike Si MOSFETs and SiC MOSFETs, GaN HEMTs do not have an intrinsic body diode. Instead, the device is able to conduct in reverse through the main 2DEG channel forming. Although the internal mechanism for reverse conduction is dramatically different, its electrical characteristics are very similar to that of a diode, with a forward voltage and a channel resistance. For ICeGaN, the forward voltage is approximately the V_{TH} of the power HEMT, assuming that V_{GS} = 0 V. The additional integrated circuitry does not impact the reverse conduction characteristics. V_{SD} is quoted as a static parameter in the table on the datasheet at a given current when V_{GS} = 0 V. Reverse voltage is also plotted against drain current for third quadrant operation in the table of figures. An example of this graph is shown below in Figure 5.
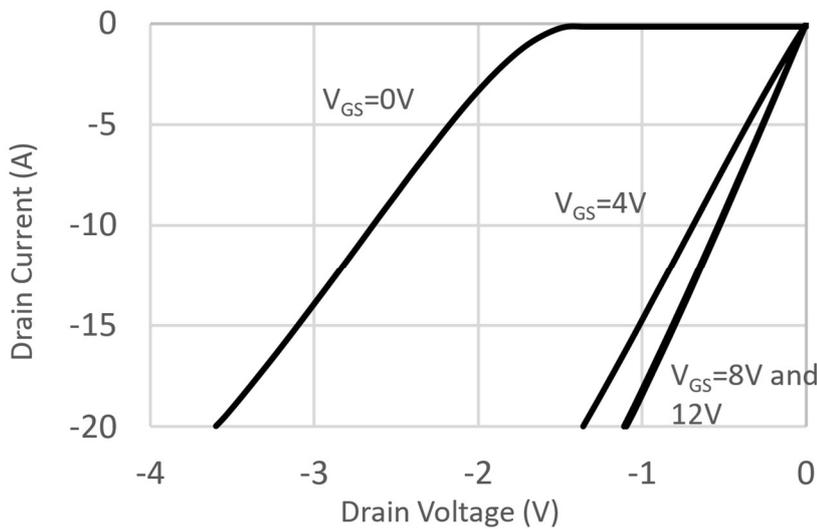

Figure 5 - Third quadrant characteristics of ICeGaN.

An advantage of ICeGaN over discrete e-GaN becomes apparent here, as if a negative voltage is required for the gate low condition, this negative voltage will be added to the GaN threshold to give the forward voltage drop. For example, if $V_{GS(off)}$ = -3 V, the forward voltage for reverse conduction will be -4.5 V (-3 V + -1.5 V). In topologies such as LLC, where negative conduction is required on every switching cycle in the deadtime, this can create an efficiency benefit for ICeGaN over discrete e-GaN. ICeGaN never requires a negative voltage on the gate.

3.1.5 ESD Rating

ICeGaN has integrated ESD protection that is rated to 2 kV for Human Body Model (HBM). This protection is on all the device pins.

3.2 Driving ICeGaN

In this section we look at the switching behaviour of ICeGaN devices, specifically, the turn-on event. A 55-mΩ ICeGaN H2 series device is used in half-bridge configuration, and the switching transitions are observed in SPICE simulations (the SPICE model version is 0.1). Spice simulations have been selected for this section rather than measurements, as this allows us to
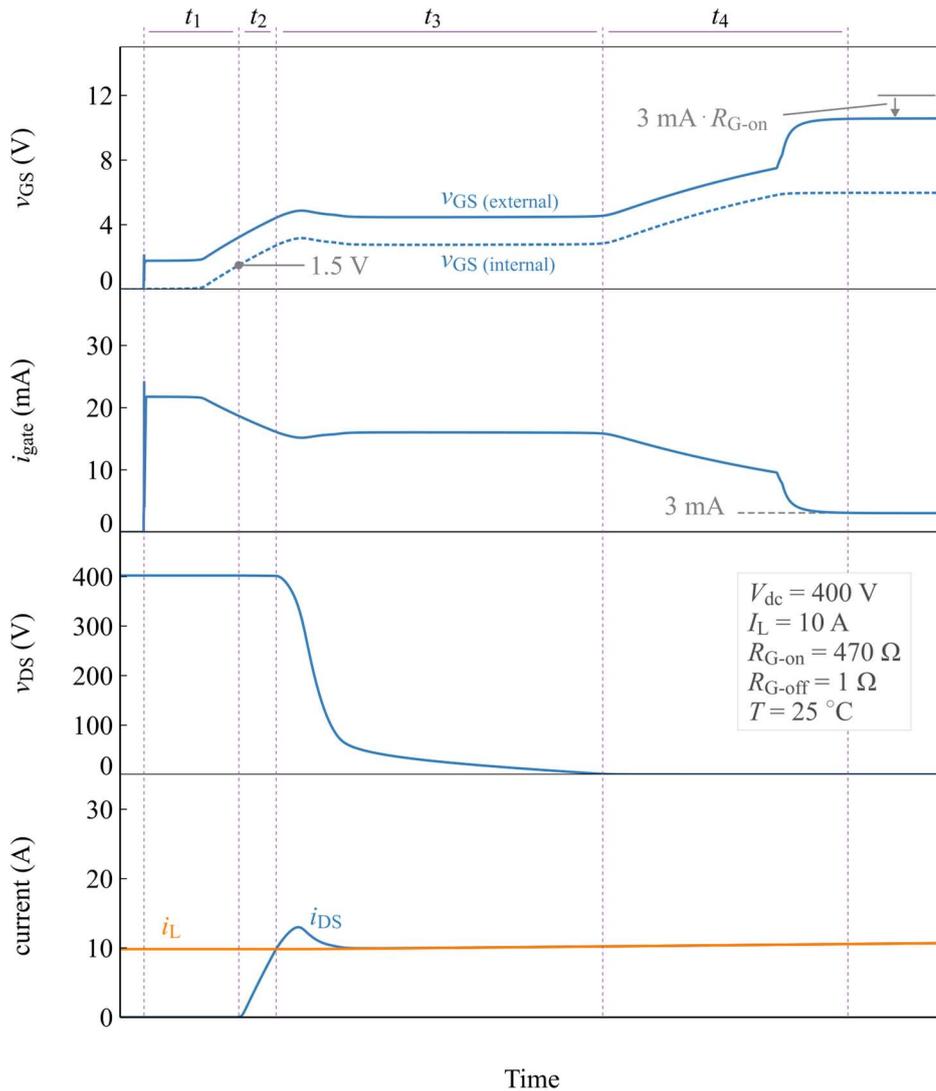
have ideal circuit conditions to isolate the switching behaviour of the ICeGaN. In later sections, switching behaviour from measurements will be shown.

The test circuit is a double pulse test configuration as shown in Figure 6. The device under test (DUT) is the low-side device S_1; the high side device is denoted as S_2. S_2 is switched complementarily to the DUT according to double pulse timing signals, although this gate driving has been omitted from the schematic for simplicity. The input dc-link voltage (V_{dc}) is 400 V. The load inductance is 120 µH, and the timing is arranged such that the test load current (i_L) is 10 A at the device turn-on. The external turn-off gate resistance (R_{G-off}) is 1 Ω for both S_1 and S_2.

We consider cases of external turn-on gate resistances, R_{G-on}:

1. R_{G-on} = 470 Ω to slow down the dynamics and provide a qualitative view on the transitions, especially the gate voltage and current.

2. R_{G-on} = 10 Ω to illustrate the switching behaviour under practical switching speeds for GaN devices.

Note that, for a given case, S_1 and S_2 have the same R_{G-on} value. V_{DD} supply and the high-state gate voltage ($V_{GS(high)}$) both are 12 V as shown in Figure 6. Operation at room temperature (T = 25 °C) is considered in the simulation.

The resulting waveforms for the DUT are shown in Figure 7 and Figure 8 for R_{G-on} = 470 Ω and R_{G-on} = 10 Ω, respectively. The gate–source voltage (external gate voltage $v_{GS(external)}$ in solid blue and internal gate voltage $v_{GS(internal)}$ in dashed blue), current flowing into the external gate terminal (i_{gate}), drain–source voltage (v_{DS}), device drain–source current (i_{DS}), and load current (i_L) are shown.

Figure 6 – Half-bridge double pulse test circuit.

Figure 7 – Simulated waveforms (in SPICE) illustrating the turn-on event of a 55-mΩ ICeGaN H2 series device. The DUT is the low-side device in Figure 6. A very high $R_{G\text{-}on}$ is used in this example to obtain qualitative behaviour of the device.

The turn-on events can be understood through four phases: t_1, t_2, t_3, and t_4. Please note that inductor current i_L will be referred to as I_L during the full switching transition, as it can be considered a constant through this short period.

3.2.1 Duration t_1

At the start of this phase, the gate-driver output signal transitions to a high-state (12 V) and a gate current starts to flow into the external gate terminal.

After the Miller Clamp is deactivated, the gate capacitance of the power HEMT is subjected to charging and we can observe $v_{GS(internal)}$ starts to increase from 0 V. This phase ends when $v_{GS(internal)}$ reaches the threshold voltage of the power HEMT, which is around 1.5 V in the simulation model. At this point, the device channel starts to conduct and we can observe i_{DS} begin to rise at the end of t_1.

3.2.2 Duration t_2

This period is the time it takes for i_{DS} of S_1 to rise from 0 A to I_L (the device channel of S_1 is active, however, not fully enhanced). At the same time the current in S_2, which flows from its source to drain, starts to fall from 10 A to 0 A. In other

words, during this period, the load current I_L is shared between S_1 and S_2, such that $i_{DS,S1}$+ $(-i_{DS,S2})$ = I_L. Note that during both t_1 and t_2, v_{DS} is clamped at the dc-link voltage of 400 V: therefore, no currents related to charging/discharging of device output capacitances flow in this stage.
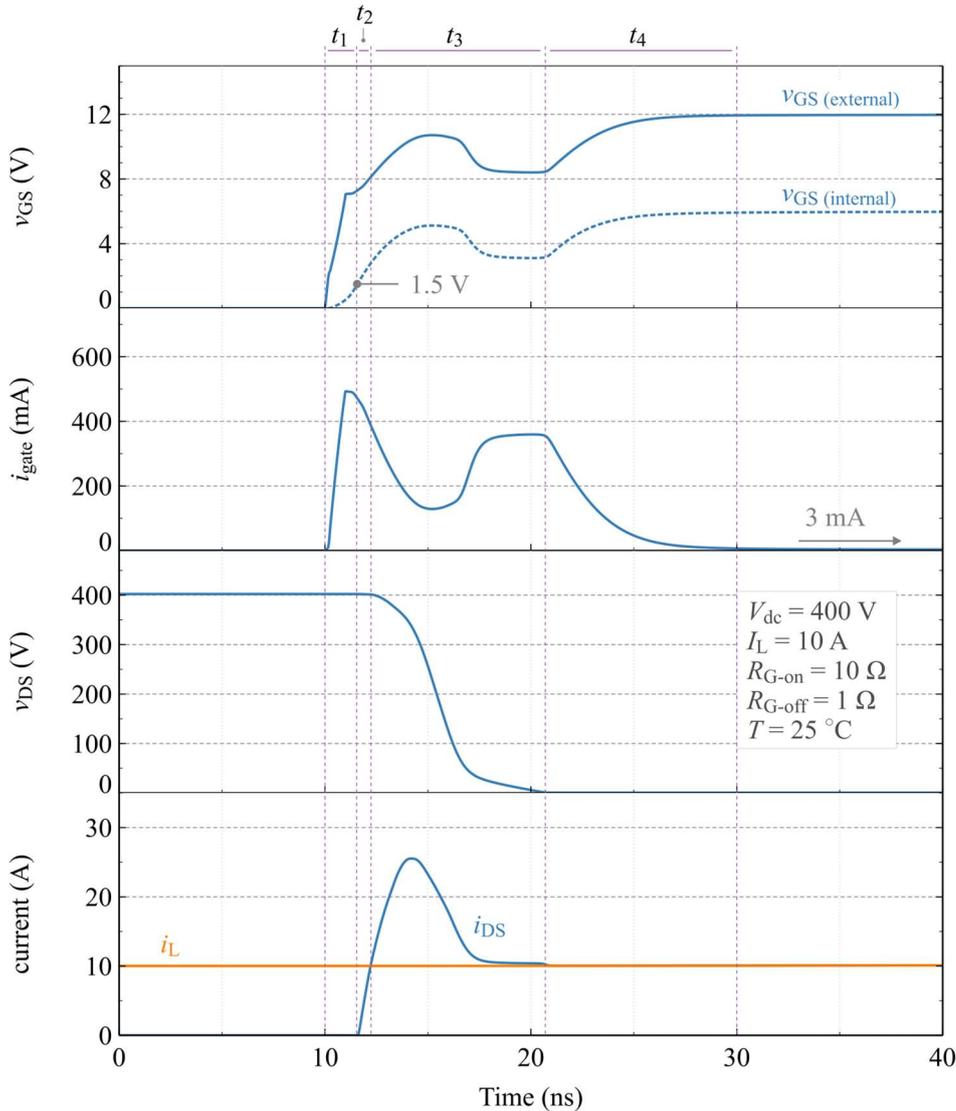
Figure 8 – Simulated waveforms (in SPICE) illustrating the turn-on event of a 55-mΩ ICeGaN H2 series Device. Compared to Figure 7, an R_{G-on} of 10 Ω is used in this example to demonstrate the device behaviour at practical turn-on speeds.

3.2.3 Duration t₃

This is the drain–source voltage fall period of S_1 (drain–source voltage rises in S_2 simultaneously). The output capacitance (C_{OSS} = C_{GD}+C_{DS}) of S_1 gets discharged through the channel of S_1: this current circulates internally between output capacitance and device channel, and therefore cannot be observed in external device drain–source current measurements. At the same time the output capacitance of S_2 gets charged (from 0 V to V_{dc}) by the power source V_{dc}, through the channel of S_1; this is the reason why i_{DS} of S_1 exceeds I_L for a certain amount of duration as it needs to facilitate both I_L and the charging current of the output capacitance of S_2. During this period, both $v_{GS(external)}$ and $v_{GS(internal)}$ of S_1, are in the conventionally known plateau region, although we see a peak and a trough due to fast transition times of GaN devices [14].

3.2.4 Duration t$_4$

At the onset of this phase, v$_{DS}$ of S$_1$ has reached approximately zero (strictly the product of the device R$_{DS}$ and its current i$_{DS}$ at that time). Gate–source voltages reach their final on-state values: v$_{GS(external)}$ will settle to V$_{GS(high)}$ − i$_G$ · R$_{G-on}$ (in Figure 7, this is around 10.6 V due to large R$_{G-on}$, and in Figure 8, this is ~ 12 V as R$_{G-on}$ is small) and v$_{GS(internal)}$ gets clamped at ~5 V irrespective of the value of R$_{G-on}$. At v$_{GS(internal)}$ ≈ 5 V, the channel of S$_1$ is fully enhanced. The on-state gate current further reduces and settles to 3 mA at the end of this period; this 3 mA current is utilised by the ICeGaN circuitry to support the functioning of its current source and the voltage limiter circuits.

3.3 Controlling of the Switching Speed

This subsection will focus on the turn-on and turn-off switching speeds of ICeGaN devices. We concern ourselves with purely experimental results in this section and utilise the half-bridge circuit diagram in Figure 6 to carry out double-pulse testing with one major difference: the high-side device S$_2$ does not switch and operate in diode mode by shorting its gate terminal to Kelvin terminal. The ICeGaN half-bridge evaluation board is CGD-ASYEVB00701-01 [15]. The tests were carried out at V$_{dc}$ = 400 V, T$_{amb}$ = 25 °C, I$_L$ = 11 A (the inductor current i$_L$ can be considered to be fixed at I$_L$ = 11 A). A Skyworks SI8271 gate-driver IC was used to drive the DUT (S$_1$).

3.3.1 Turn-on Speed

In general, the turn-on speed of ICeGaN devices can be controlled by either changing the turn-on gate resistance R$_{G-on}$, or the high-state gate voltage (V$_{GS(high)}$). In practice, the maximum turn-on speed that can be achieved is limited by the gate-driver source current capability.

While not expected to impact the results, in the testing, the turn-off resistor of the DUT was kept fixed at 2.2 Ω for consistency. First, the effect of R$_{G-on}$ of S$_1$ is evaluated. The following values of R$_{G-on}$ were considered to show its effect on turn-on slew rate (or dv$_{DS}$/dt): 2.2 Ω, 4.7 Ω, 10 Ω, 22 Ω, 47 Ω, and 100 Ω. The dv$_{DS}$/dt of the DUT was measured between 90% and 10% of V$_{dc}$. Figure 9 shows the experimental double pulse test (DPT) waveforms for two different R$_{G-on}$ values (10 Ω and 100 Ω), where V$_{GS(high)}$ was fixed at 12 V. A zoomed view of the turn-on transitions for these two cases are given in Figure 10: dv$_{DS}$/dt values of 60 V/ns and 23.4 V/ns were observed for R$_{G-on}$ = 10 Ω and 100 Ω, respectively. The full results of dv$_{DS}$/dt values are tabulated in Table 5.

Subsequently, the effect of V$_{GS(high)}$ on turn-on slew rate is considered: values of V$_{dd}$ = V$_{GS(high)}$ = 9 V, 12 V, 20 V were considered while R$_{G-on}$ was kept fixed at 47 Ω. Experimental waveforms are plotted in Figure 11, for V$_{GS(high)}$ = 12 V and 20 V. It is observed that dv$_{DS}$/dt increases from 37 V/ns to 61 V/ns by increasing V$_{GS(high)}$ from 12 V to 20 V. The results for all three V$_{GS(high)}$ values are summarised in Table 6. Note that, for low R$_{G-on}$ values (in general, values below 20 Ω), the effect of V$_{GS(high)}$ on turn-on dv$_{DS}$/dt will be much less than that at large R$_{G-on}$ values, such as 47 Ω we have considered above. This is partly because, at low R$_{G-on}$ values, the turn-on dv$_{DS}$/dt is limited by the gate-driver source-current capability.
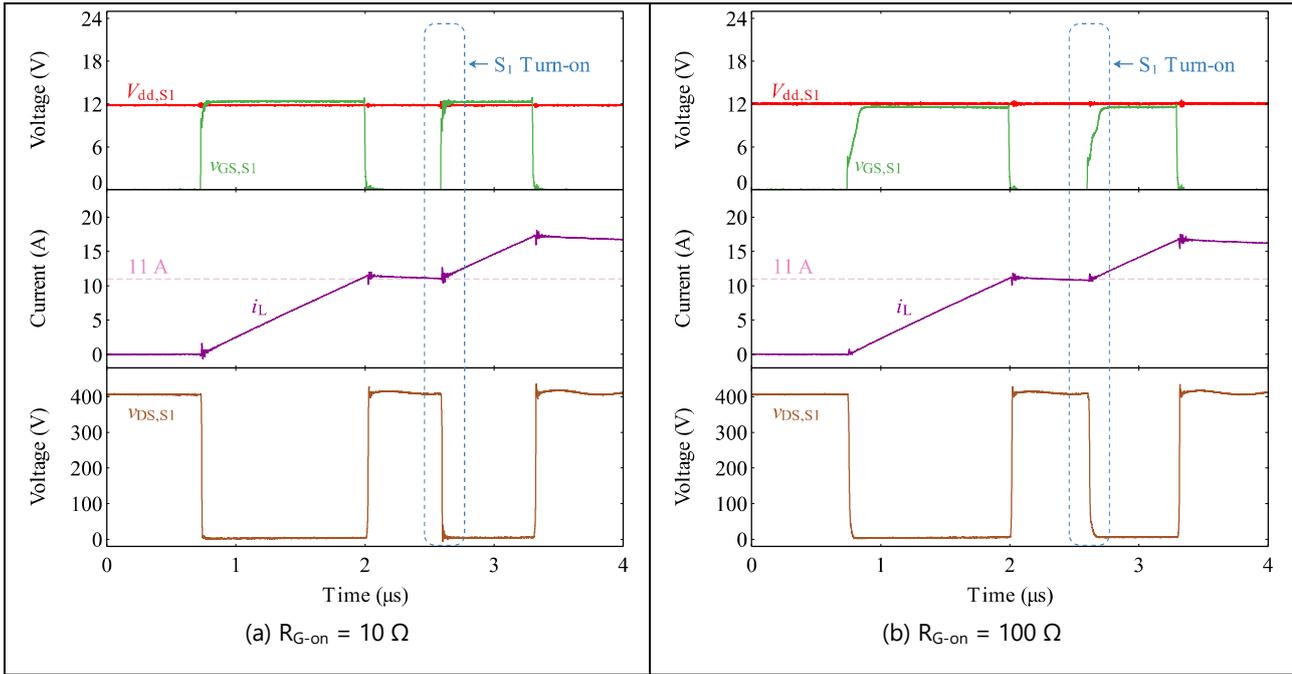
Figure 9 – 55 mΩ ICeGaN H2 series experimental waveforms in a double pulse test for two different $R_{G\text{-}on}$ values. S_1 was the DUT, and S_2 was operated in diode mode by keeping its V_{GS} = 0 V. Test Conditions: V_{dc} =400 V; I_{load} = 11 A; V_{dd} = $V_{GS(high)}$ = 12 V; $R_{G\text{-}off}$ = 2.2 Ω; T = 25 °C.
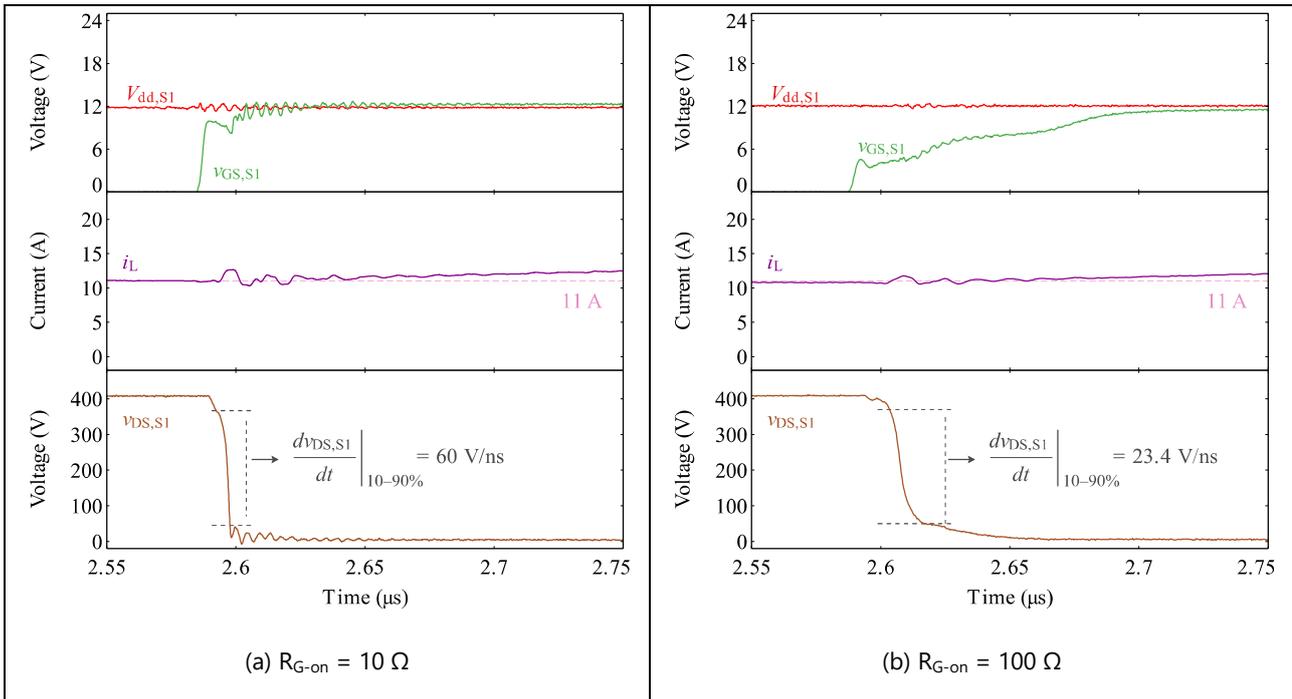

Figure 10 – Zoomed in waveforms showing the turn-on events corresponding to Figure 9 (a) and Figure 9 (b).

$R_{G\text{-}on}$ (Ω)	2.2	4.7	10	22	47	100
dv_{DS}/dt (V/ns)	61.5*	61.3*	60.1	51.6	37.1	23.2

Table 5 – dv_{DS}/dt (90% to 10% of V_{dc}) measurement summary under different $R_{G\text{-}on}$, where V_{drive} = V_{dd} =12 V.

* Limited by gate driver source current.

| (a) V_{dd} = V_{drive} = 12 V | (b) V_{dd} = V_{drive} = 20 V |
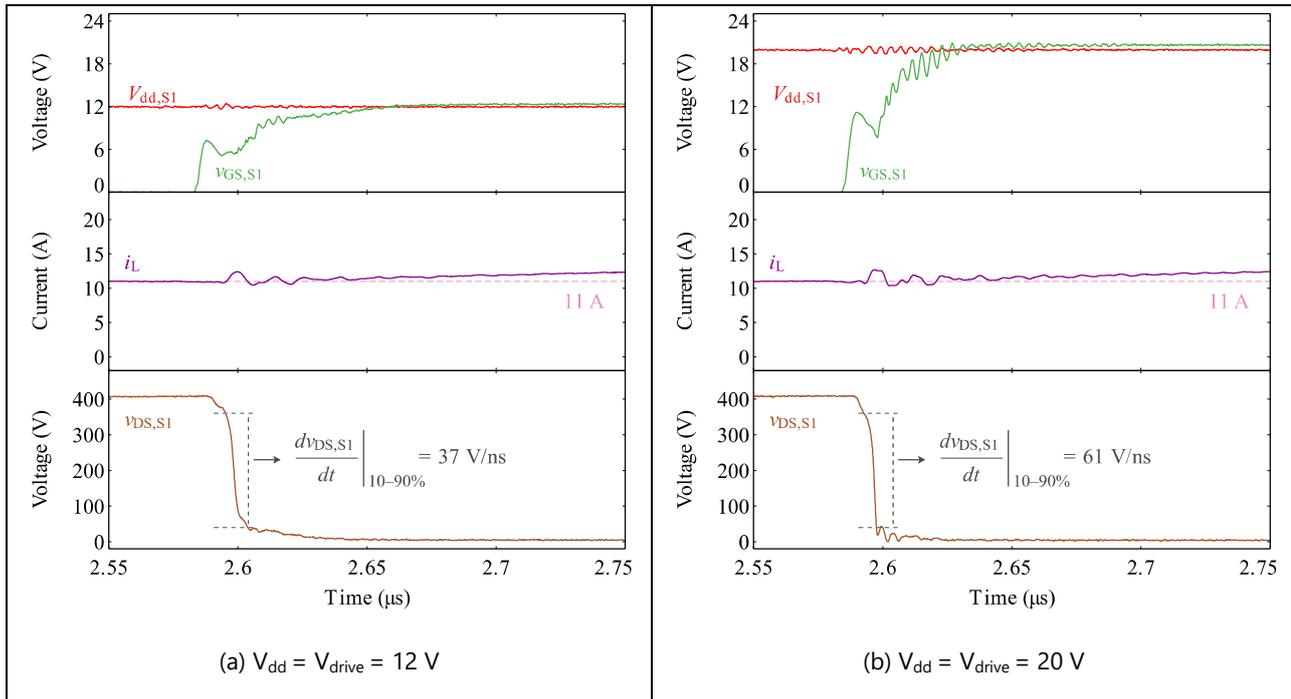
Figure 11 – 55 mΩ H2 series ICeGaN experimental turn-on waveforms for two different $V_{GS(high)}$ (= V_{dd}) values. Test Conditions: V_{dc} =400 V; I_{load} = 11 A; R_{G-on} = 47 Ω. R_{G-off} = 2.2 Ω; T = 25 °C.

V_{drive} (V)	dv_{DS}/dt (V/ns)
9	17
12	37.1
20	61

Table 6 – dv_{DS}/dt (90% to 10% of V_{dc}) measurement summary under different $V_{GS(high)}$ (= V_{dd}), where R_{G-on} is fixed at 47 Ω.

3.3.2 Turn-off Speed

For discrete HEMTs, the turn-off gate resistance R_{G-off}, determines the v_{GS} fall time, and hence the channel cut-off time. The voltage rise time of v_{DS}, or equivalently turn-off dv_{DS}/dt, is predominantly determined by load current in half-bridge configurations. Note, that strictly in this case the turn-off gate resistance will be the parallel combination of R_{G-on} and R_{G-off}. Typically R_{G-off} < R_{G-on} and as such an approximation is made that the turn-off resistance is solely determined by R_{G-off}. This assumption will be made in this document.

In contrast, in ICeGaN devices, although the external v_{GS} fall time is determined by R_{G-off}, the channel cut-off time is determined by the internal Miller Clamp, and is largely independent of R_{G-off}. Then, as with discrete HEMTs, the voltage rise time of v_{DS} and turn-off dv_{DS}/dt, is determined by the load current.

In Figure 12, experimental turn-off transitions for two R_{G-off} values are plotted: (a) R_{G-off} = 2.2 Ω and (b) R_{G-off} = 100 Ω. The results show that, first, the external v_{GS} fall time increases as R_{G-off} in increased. This consequently increases the total turn-

off delay time (defined as the time duration between 90% of v_{GS} and 90% of v_{DS} as illustrated in Figure 12). On the other hand, by observing v_{DS} waveforms, we also verify that the turn-off dv_{DS}/dt is fairly independent of $R_{G\text{-off}}$.

Table 7 summarises turn-off delay times for several $R_{G\text{-off}}$ values and $V_{GS(high)}$ values. It is observed that for $R_{G\text{-off}}$ of 10 Ω and below, the turn-off delay times are relatively fixed around 23–25 ns for this specific device, and no clear effect on $R_{G\text{-off}}$ and $V_{GS(high)}$ are observed.

CGD recommends to always use low $R_{G\text{-off}}$ to accelerate the channel cut-off and to keep the turn-off delay time as small as possible.
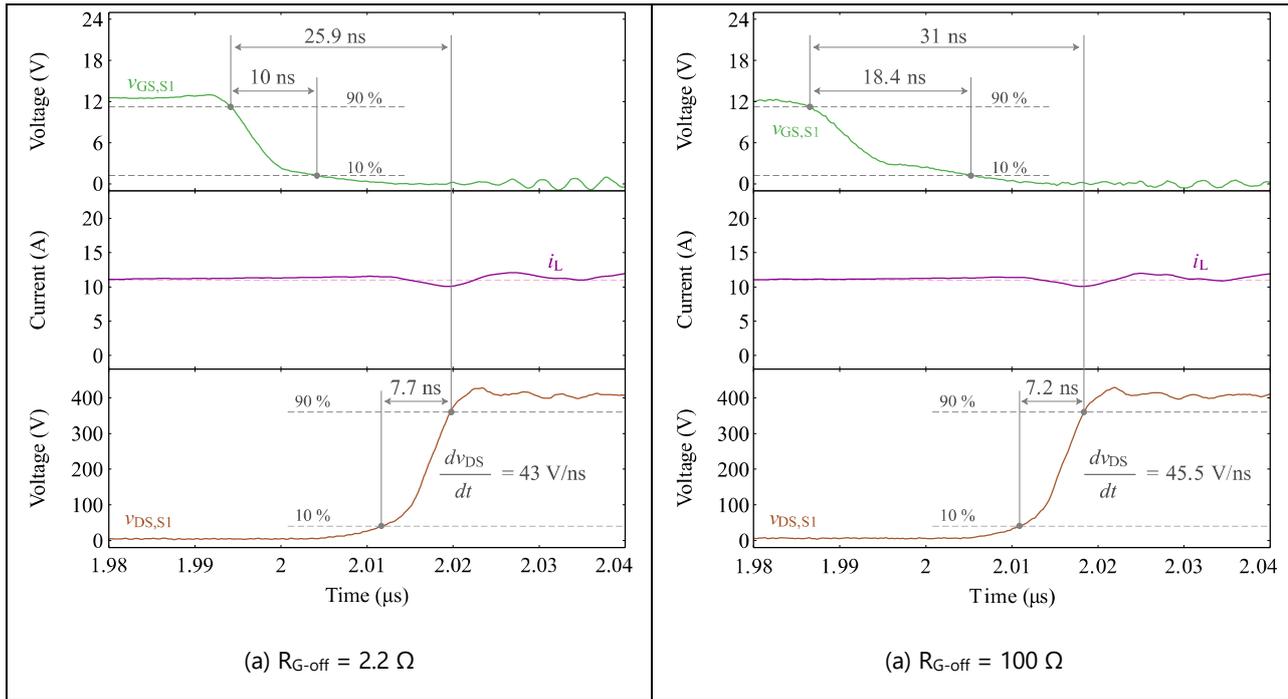
Figure 12 – Turn-off waveforms under different $R_{G\text{-off}}$ values and same $R_{G\text{-on}}$ of 10 Ω. Test Conditions: V_{dc} =400 V; I_{load} = 11 A; V_{dd} = V_{drive} = 12 V; T = 25 °C.

V_{drive} (V)	Turn-off delay time (ns)				
	$R_{G\text{-off}}$ = 1 Ω	$R_{G\text{-off}}$ = 2.2 Ω	$R_{G\text{-off}}$ = 4.7 Ω	$R_{G\text{-off}}$ = 10 Ω	$R_{G\text{-off}}$ = 100 Ω
9	24.4	24.2	24.1	24.6	29.6
12	25.5	25.9	25.3	25.6	31
20	23.7	25.4/25.8	23.7	24.8	30.5

Table 7 – Summary of turn-off delay times (from 90 % of v_{GS} to 90 % of v_{DS}) measurements for different $R_{G\text{-off}}$ and $V_{GS(high)}$ (= V_{dd}). Test conditions: V_{dc} =400 V; I_L = 11 A; $R_{G\text{-on}}$ = 10 Ω; T = 25 °C.

3.4 Powering ICeGaN Through V$_{DD}$

ICeGaN requires a constant voltage to be supplied to its VDD pin for proper operation of the device. This supply is used to power the integrated circuitry and maintain the on state of the Miller clamp while the gate is low. The consumption of this

pin in various states has been discussed in Chapter 3.1.3 when the VDD pin has already reached its steady-state value. For ease of reading, Table 4 has been repeated below as Table 8. CGD typically recommends a small decoupling capacitor to be fitted close to the VDD pin of the device. The standard value suggested is 100 nF. This capacitor should be fitted between VDD and K pins.

The adaptive power consumption mechanism, NL^3 circuit, enables a significant reduction in current draw during the idle state. This enables ICeGaN to be utilised in circuits that need to meet the increasingly stringent no-load and low-load power consumption requirements.

ICeGaN H2 series requires a maximum of 250 µA during start-up. If the VDD pin is common with the controller/gate driver VCC, this current should be considered when calculating the start-up time and current requirements. ICeGaN H1 series will require additional start-up current by comparison, and it should be assumed the current requirement is equal to the steady state value listed on the respective datasheet.

Parameter		Conditions	Min	Typ	Max	Unit
V_{DD} Current (V_{GS} in on-state)	I_{VDD}	V_{GS} = 12 V, V_{DS} = 0 V		1	1.6	mA
V_{DD} Current (V_{GS} in on-state)	I_{VDD}	T_J = 150 ºC, V_{GS} = 12 V, V_{DS} = 0 V		0.5		mA
V_{DD} Current (V_{GS} in off-state)	I_{VDD}	V_{GS} = 0 V, V_{DS} = 0 V		70	150	µA
V_{DD} Current (V_{GS} in off-state)	I_{VDD}	T_J = 150 ºC, V_{GS} = 0 V, V_{DS} = 0 V		35		µA
V_{DD} Start-up Current	I_{VDD_start}	V_{GS} = 0 V, V_{DS} = 0 V		250		µA

Table 8 - V_{DD} current consumption for CGD65A055SH2.

3.5 Alternative Means of Supplying V$_{DD}$

In low power applications, such as a universal input voltage ac to dc flyback converter, the supply voltage of the controller may be higher than 20 V, making it incompatible with the ICeGaN VDD pin. This means the controller supply voltage would need to be stepped down before it could be supplied to VDD. This adds extra components and could affect the no-load performance of the SMPS. One possible solution to this is to provide the V$_{DD}$ voltage through the gate signal. An example of such an implementation is drawn in Figure 13.
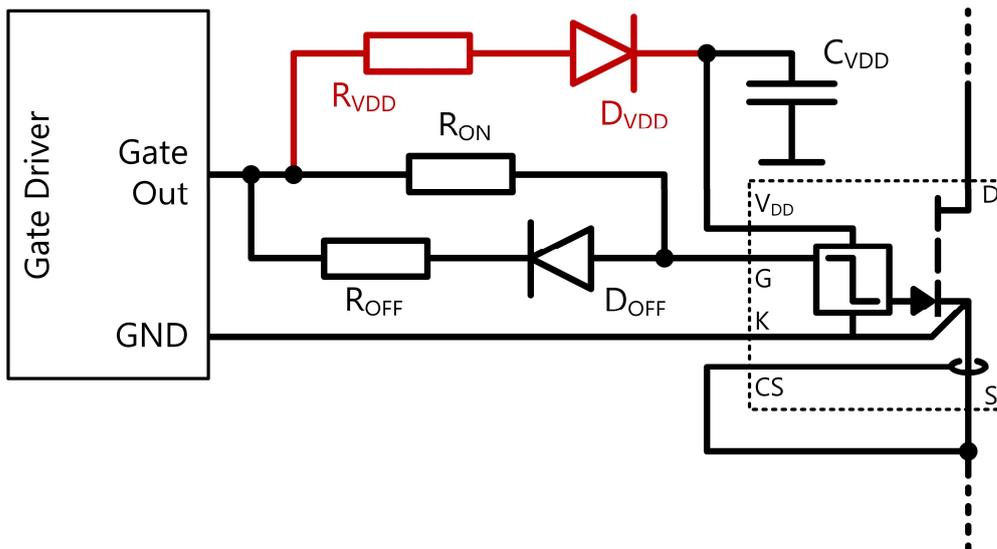
Figure 13 - ICeGaN configuration where VDD is driven from gate signal through R$_{VDD}$ and D$_{VDD}$.

The behaviour is similar to that of a bootstrap circuit. When the gate is high, D$_{VDD}$ is forward biased, and C$_{VDD}$ will charge through current supplied by the gate driver 'Gate Out' pin. When the gate is low, D$_{VDD}$ will be reverse biased and maintain

the charge on C$_{VDD}$. Simplified circuits of these two operating modes are shown in Figure 14. These simplified circuits will aid in calculating the required values of R$_{VDD}$, C$_{VDD}$, minimum charging time (t$_{min}$) and maximum discharge time (t$_{max}$). It is assumed in these calculations that the supply from the gate driver is limitless. This is a reasonable assumption as gate drivers can typically provide several Amps of current, far more than this circuit and the ICeGaN will require in steady state.
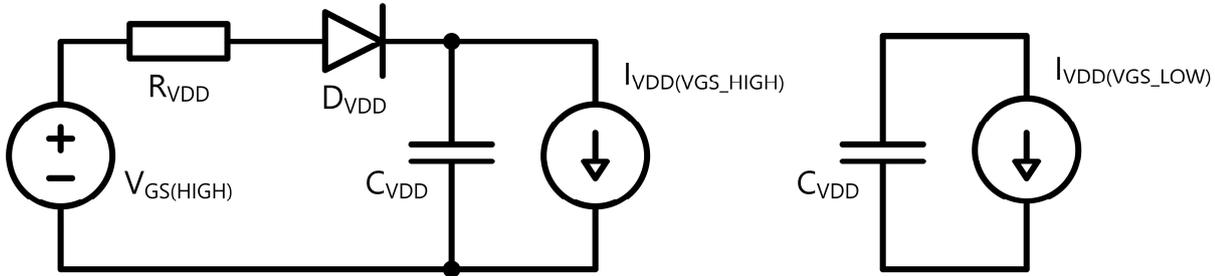
Figure 14 - Simplified circuit of V$_{DD}$ charging operating modes with V$_{DD}$ powered from gate pin.

(Left: V$_{DD}$ charging when gate is high. Right: V$_{DD}$ discharging when gate is low).

The minimum time to charge C$_{VDD}$ from 0 V to V$_{DD1}$ can be calculated by the equation below. Note: V$_{DD1}$ is intended to be a voltage > 9 V such that V$_{DD}$ is in its operational range. The calculated examples will set this to 10 V to allow for 1 V discharge between the subsequent gate pulse. This value should be set on a circuit-by-circuit basis. V$_F$ is the forward voltage of D$_{VDD}$ and V$_{GS\_HIGH}$ is the gate voltage in the on state.

$$t_{min} = -ln\left(\frac{V_{DD1} - V_{GS_{HIGH}} + R_{VDD}I_{VDD(VGS_{HIGH})} + V_F}{-V_{GS_{HIGH}}}\right)R_{VDD}C_{VDD}$$

The maximum time to discharge V$_{DD}$ to 9 V is given by the equation below. Note: V$_{DD2}$ is the voltage on C$_{VDD}$ at the end of the charging cycle in a steady state condition.

$$t_{max} = \frac{C_{VDD}(V_{DD2} - 9V)}{I_{VDD(VGS_{LOW})}}$$

The circuit parameters must be carefully chosen based on the typical operating conditions of the SMPS, but also the atypical cases such as burst mode and start up.

For single ended topologies such as quasi-resonant (QR) flyback, V$_{DD}$ is only required for the gate turn-off and any significant dv/dt on the drain, likely caused by idle rings. This means the V$_{DD}$ can deplete during idle periods where no device switching occurs, such as during burst modes. In half bridge topologies, this allowance cannot be made, as the complimentary device can cause a significant dv/dt on the drain, and a spurious turn-on for the non-switching device. In these environments, the capacitor on the VDD pin should be sized such that V$_{DD}$ can never deplete.

An example will be given with values for CGD65B240SH2 (240 mΩ ICeGaN H2 series). It is recommended to use the maximum I$_{VDD}$ current at 25 °C. For CGD65B240SH2, this is 1.4 mA when the gate is high and 150 µA when the gate is low.

Parameter		Conditions	Min	Typ	Max	Unit
V$_{DD}$ Current (V$_{GS}$ in on-state)	I$_{VDD}$	V$_{GS}$ = 12 V, V$_{DS}$ = 0 V		0.8	1.4	mA
V$_{DD}$ Current (V$_{GS}$ in on-state)	I$_{VDD}$	T$_J$ = 150 °C, V$_{GS}$ = 12 V, V$_{DS}$ = 0 V		0.4		mA
V$_{DD}$ Current (V$_{GS}$ in off-state)	I$_{VDD}$	V$_{GS}$ = 0 V, V$_{DS}$ = 0 V		70	150	µA
V$_{DD}$ Current (V$_{GS}$ in off-state)	I$_{VDD}$	T$_J$ = 150 °C, V$_{GS}$ = 0 V, V$_{DS}$ = 0 V		35		µA
V$_{DD}$ Start-up Current	I$_{VDD\_start}$	V$_{GS}$ = 0 V, V$_{DS}$ = 0 V		250		µA

Table 9 – V$_{DD}$ current consumption for CGD65B240SH2.

Below are graphs for selecting appropriate R_{VDD} and C_{VDD} values based on the required minimum charge time and maximum discharge time.
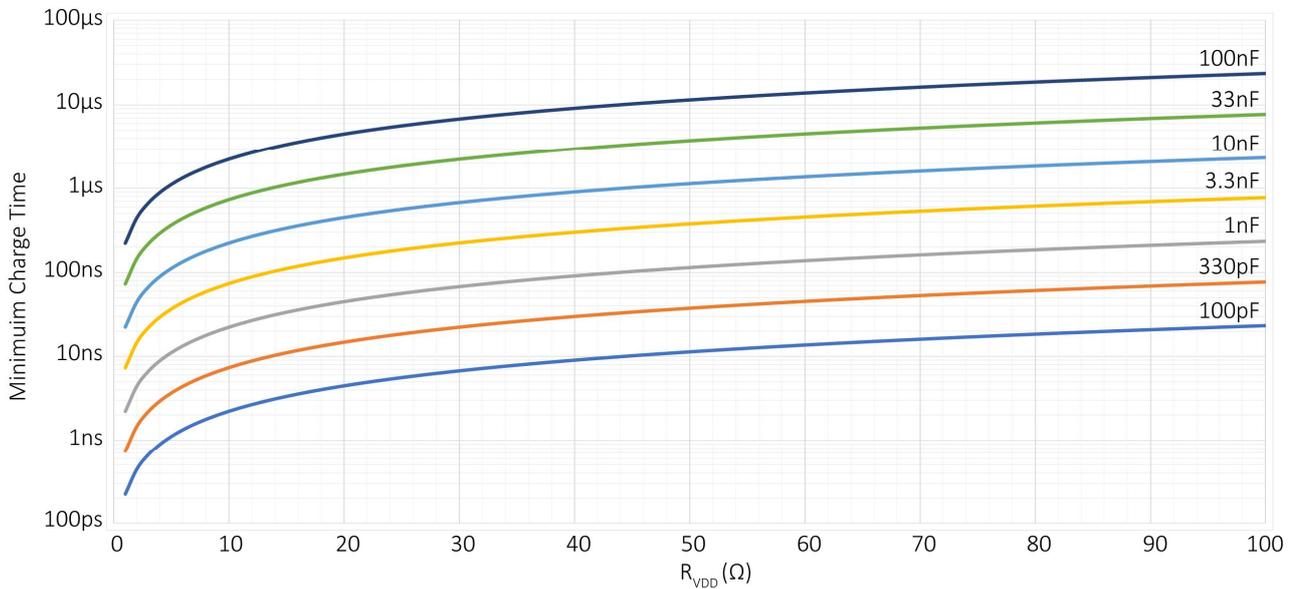

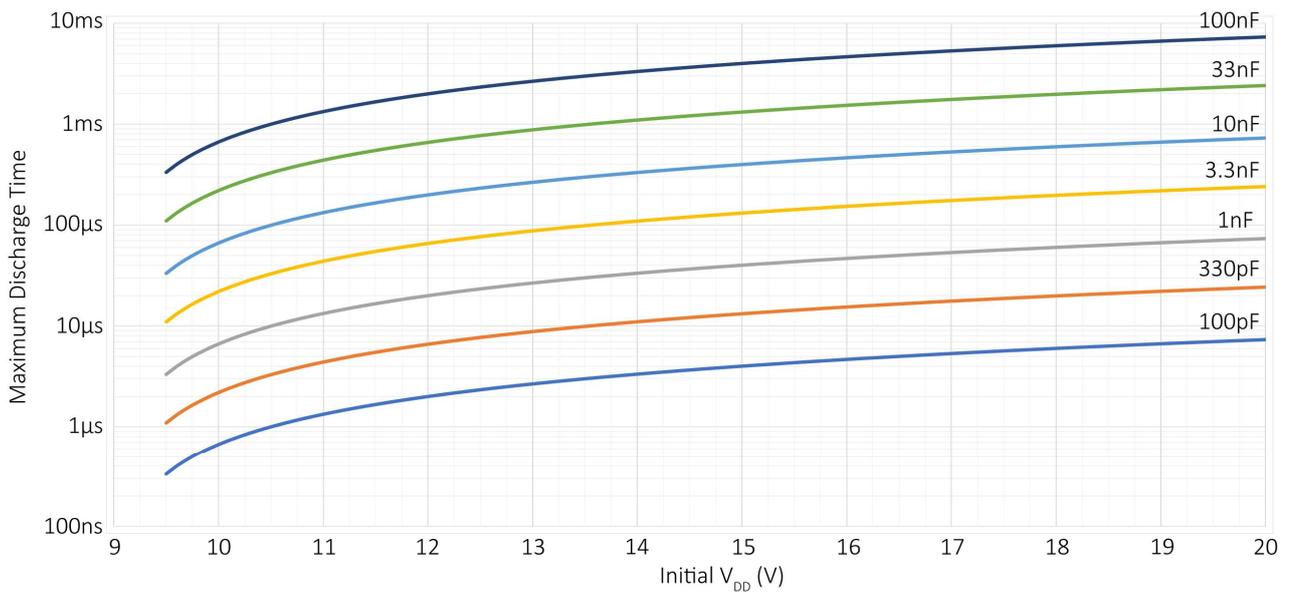*Figure 15 - Minimum charging time to 10 V for various R_{VDD} and C_{VDD} values.*

Figure 16 - Maximum discharging time to 9 V V_{DD} for various initial V_{DD} and C_{VDD}.

To show this circuit working within an application, a 65 W QR flyback converter [16] has been modified to include the ICeGaN VDD pin being powered through the gate. In the example, CGD65B240SH2 has been utilised with R_{VDD} = 10 Ω, C_{VDD} = 10 nF, and 30 V Schottky diode PMEG3005EJ as D_{VDD}. Typically, it would be the recommendation of CGD to use a Schottky diode for D_{VDD}. The QR flyback design utilises the NCP1342 controller which directly drives the gate of the ICeGaN with a maximum 500 mA source current.

Below, Figure 17 shows the behaviour during start up. The selected condition is a no-load start up, as this should be the worst case for minimal gate pulses. It can be seen that while the VDD pin is not able to fully establish in the first pulse due

to how narrow it is in this no load condition, it has fully established from the third pulse. At no subsequent point during the start up does the VDD pin drop below the required 9 V, even with significant periods of gate being low.
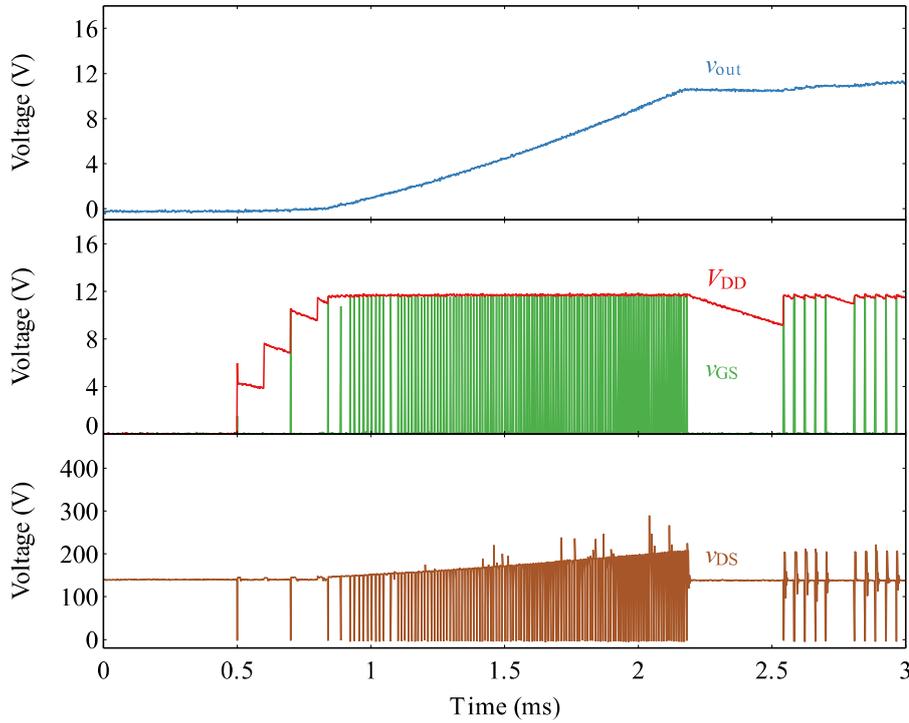
Figure 17 - V_{DD} behaviour through start up in no-load.
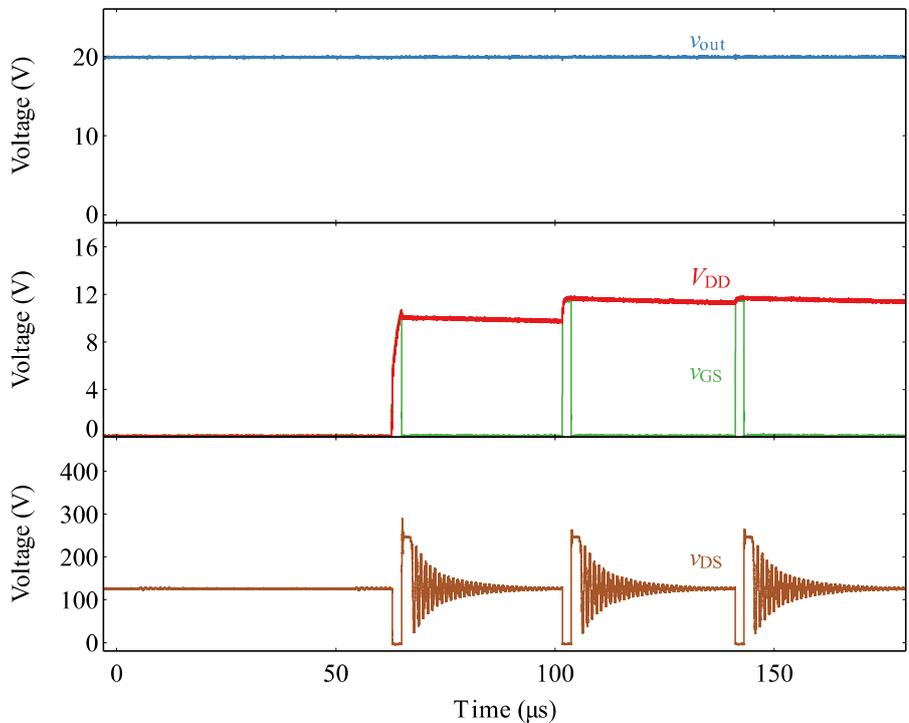
Figure 18 - V_{DD} behaviour during burst mode.

Above in Figure 18 is the behaviour out of burst mode in no-load. It can be seen that in the long idle period prior, the V_{DD} fully depletes as there were not any gate pulses. The first gate pulse is sufficient to charge the VDD pin back up, and

maintain being high through the subsequent off period within the burst period. Given this is a single ended topology, V_{DD} is not required to maintain the device in an off state while the SMPS is idle, since there is no secondary device that can create a dangerous dv/dt on the drain and cause a spurious turn-on event. If this was a half bridge topology, additional care would need to be taken, and the capacitor C_{VDD} would likely need to be larger. Ordinarily, CGD would not recommend this approach for half bridge topologies, it would be better to share V_{DD} with the high side driver supply through a bootstrap.

Finally, below in Figure 19 the performance is shown in a normal operating condition, specifically 10% load. V_{DD} can easily be maintained in this light load, continuous switching condition.
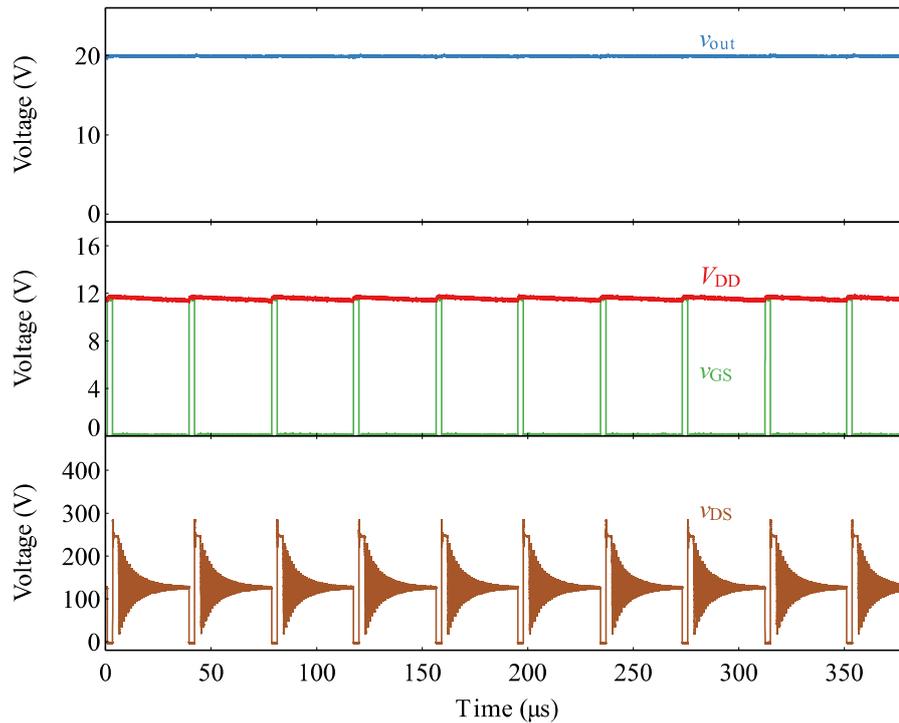
Figure 19 - V_{DD} behaviour in 10% load condition.

3.6 Current Sense

As discussed in detail in section 2.2.4, the current sense pin provides a current output proportional to the drain current of the device. CGD-AN2206 [17] discusses how to best use this current output, and it is advised to refer to this document before implementing a circuit that utilises the CS pin.

It should be noted that if the CS pin is unused, it should be connected directly to device source.

4 Conclusion

E-mode GaN HEMTs offer improved switching performances over SJ SiMOS and SiCMOS. These HEMTs are best suited to use in continuous hard-commutated half-bridge-based topologies, such as totem-pole boost converter; and high switching frequency in resonant zero-voltage-switching topologies, such as LLC. They allow design engineers to push their Switch Mode Power Supplies further than previously possible with regards to frequency, efficiency, and power density. However, the low threshold voltage and the narrow range of V_{GS} make the discrete e-mode GaN HEMTs difficult to use in such designs. To overcome these two problems Cambridge GaN Devices (CGD) provides an ease-of-use solution, ICeGaN. ICeGaN has a built-in Miller Clamp for turn-off, eliminating the need for negative voltages to keep the gate off. In addition, the integrated auxiliary HEMT increases the threshold voltage of the device and provides a wider operating voltage range. These two together improve the immunity of ICeGaN to dv/dt-related parasitic turn-on events, ensuring reliable turn-on and turn-off of the device, and make the GaN HEMT compatible with widely available gate drivers, originally designed for MOSFETs or IGBTs. Details about the ICeGaN internal functional blocks have been discussed in this application note. The key parameters of ICeGaN including V_{DD}, $V_{GS(th)}$, V_{GS}, and CS have been explained. It has been demonstrated that the turn-on waveform of ICeGaN is similar to that of a discrete e-mode GaN HEMT, and the turn-on switching speed can be controlled by a turn-on gate resistor. The CS pin provides the Power HEMT current information to a controller.

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Figures

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Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	JF	20/05/2024

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