ICeGaN™ HEMT PCB LAYOUT GUIDE

APPLICATION NOTE

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Abstract

ICeGaN™ HEMTs can provide engineers several advantages over silicon counter parts due to their superior electrical characteristics resulting in less device losses, particularly in hard switching applications, as well as having the main thermal pad being source referenced rather than drain. The combination of these two benefits enables designs that can avoid the need for external extruded heatsinks to be attached to the device for thermal management. This document will outline the steps that can be taken to optimise thermal performance when using the copper of a PCB as the only source of heatsinking. It is ultimately recommended to use a multilayer PCB with thermal vias connecting between a component side 'H' copper area and larger thermal relief beneath.

Introduction

The structure of a gallium nitride high electron mobility transistor (GaN HEMT) differs from that of a MOSFET, making it much easier to expel heat through a HEMT's source pad. Choosing the source for the main heat evacuation route changes the priorities for PCB layout and eliminates much of the compromise between thermal management and electrical performance, especially with regard to EMI (electromagnetic interference). This application note will explain how to optimize the PCB layout for thermal and electrical performance of ICeGaN™ while minimising EMI.

ICeGaN™ Overview

ICeGaN™ stands for "Integrated Circuit Enhancement GaN". It is a platform based on an enhancement GaN HEMT aimed at lowering losses and running cooler than other MOSFET solutions, due to its ultra-low specific on-state resistance and very low capacitances. Critically for an engineer, ICeGaN™ can be driven in a similar manner to a silicon MOSFET meaning that unlike all other enhancement GaN solutions it is compatible with any silicon-based driver. Its zero reverse recovery losses and very low output charge makes it an ideal choice for high frequency, high efficiency applications.

Presently there are two approaches for e-mode GaN in the market (i) discrete approach and (ii) monolithic approach where the gate driver is fully integrated. Both these solutions have their own shortcomings. The low threshold voltage *(~1.2 V for Ohmic p-GaN gate solutions and 1.7 V for Schottky p-GaN gate devices)* specific to p-GaN enhancement mode devices requires negative drive voltages to limit false turn-on events of the HEMT during high dV/dt transients. The full driver integration, on the other hand, while providing reduced parasitics, takes away the opportunity of using industry proven low-cost, high-performance silicon-based drivers, or gate drivers integrated with powerful controllers. Additionally, due to on-chip thermal coupling, the gate driver can suffer from extra losses due to the self-heating of the power device. Scaling up a fully integrated solution to higher power levels is also questionable due to gate driver losses.

In contrast, the ICeGaN™ devices have a higher threshold voltage, $V_{th} \approx 3$ V in order to suppress dV/dt related spurious turn-on events and as a result allow safer operation. Moreover, the ICeGaN™ devices can be driven with gate voltages of up to 20 V (well in excess of the standard 7 V for enhancement mode p-GaN HEMTs) without any compromise in the device transconductance or dynamic performance.

For more information on the driving of ICeGaN™ please consult our device datasheet.

ICeGaN HEMT Packages

The ICeGaN HEMTs have been designed with a large, exposed power pad to keep their junction-to-case thermal resistance, Θ_{JC}, as low as possible. These packages use the familiar 5x6 mm and 8x8 mm DFN formats common to many power MOSFETs although, unlike in a MOSFET where the large pad is connected to the drain, the exposed pad used in ICeGaN™ packages is connected to the device source. In low-side applications this allows the drain copper area to be minimised, reducing conducted and radiated EMI. For more on the packages available with CGD ICeGaN™ please refer to datasheets such as CGD65A055S2 and CGD65B200S2. [1] [2].

Figure 1 - ICeGaN in DFN5x6 Package

Figure 2 - ICeGaN in DFN8x8 Package

PCB Design for Optimal ICeGaN™ Thermal Performance

GaN HEMTs have several electrical characteristics that make them significantly less lossy then their comparable silicon counterparts. The consequence of this, is that in many cases, it is possible to heatsink the devices sufficiently into the PCB copper area such to not require additional external heatsinks. This has many potential benefits such as increased reliability, decreased manufacturing costs and higher power density designs. Further, CGD ICeGaN™ with Current Sensing allows soldering the device directly onto the ground plane without current sensing resistors compromising the thermal path. For more information on this CGD recommends referencing the white paper "Thermal Advantages of ICeGaN™" [3].

It is of course the case that the more copper dedicated to extracting the heat from ICeGaN™ source the better the thermal performance, however compromise is always needed. To maximise the benefits enabled by ICeGaN™ around these compromises, PCB design engineers can follow some advisory guidelines given in this chapter.

MAKING THE MOST OF THE TOP LAYER 'H' SHAPE

It is difficult to put a large area of copper on the same side of the PCB as the ICeGaN™. Other components are close by, as is the high voltage input net and the high voltage, high dv/dt, drain connection. All require significant creepage distance. The CGD DFN5x6 package is very similar to high power LED packages with their anodes on one side, cathodes on the other side, and an electrically isolated thermal pad in the middle as shown in Figure 3 and Figure 4. The CGD DFN8x8 has a slightly more direct path out the bottom of the device for heat sinking as can be seen from its 'L' shaped source pad in Figure 5. As a result, this subchapter will be primarily focused on the DFN5x6 but all the content can be extended to apply also ton the DFN8x8. Note, these figures have not been inserted to scale and are intended to illustrate the required paths for heat extraction from the footprint only.

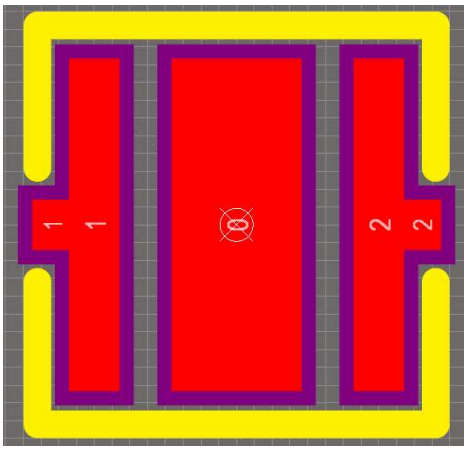

Figure 3 - Typical PCB Footprint for 3x3 Power LED

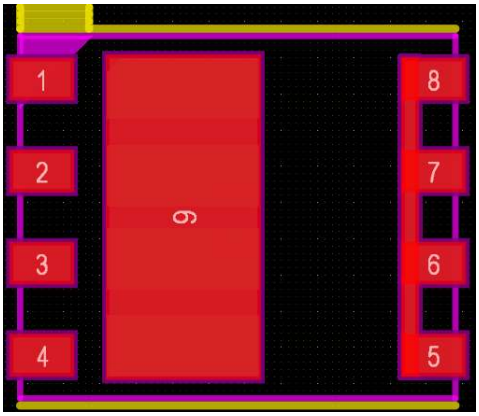

Figure 4 - Typical PCB Footprint for CGD DFN5x6

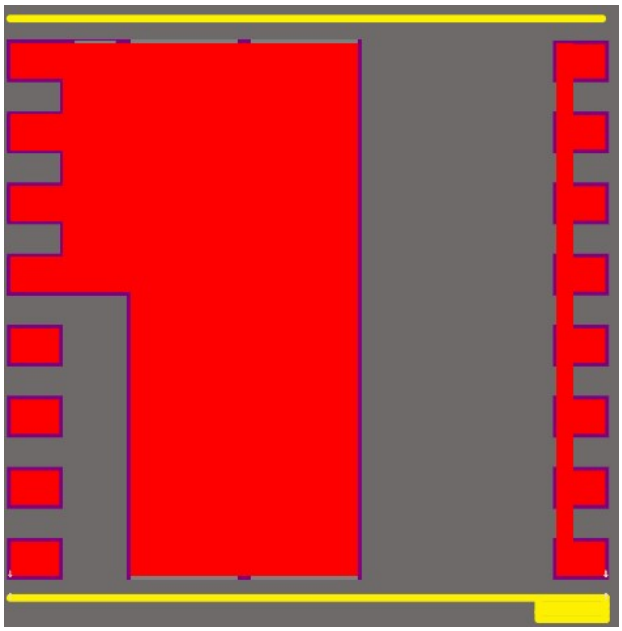

Figure 5 - Typical PCB Footprint for CGD DFN8x8

Power LEDs are often used in high volume applications with cost targets that rule out metal core PCBs. The following strategies have been developed to maximise LED thermal performance with FR-4 and can also be used with lateral GaN devices. [2]

As with most electrical insulators, FR-4 is a poor conductor of heat, so copper area is most effective on the component side. LEDs in a long series string see large DC voltages and require attention to creepage and clearance just like a HEMT. Sitting the device on the horizontal bar of an "H" shaped section of top copper, that fans out from the thermal tab, makes the most of component side copper while maintaining creepage for electrical safety.

As demonstrated in [2] and [3], there is a point of diminishing returns for copper area due to heat spreading effects. For the power LEDs on 1.6 mm-thick FR-4, extending the ends of the "dog bone" more than 4-5 mm from the thermal tab provides little reduction in thermal resistance. Increasing copper thickness also hits a point of diminishing returns above 70 µm. Figure 6 shows the suggested

orientation and minimum dog bone shape for the copper layer on the same side as an ICeGaN™ DFN5x6.

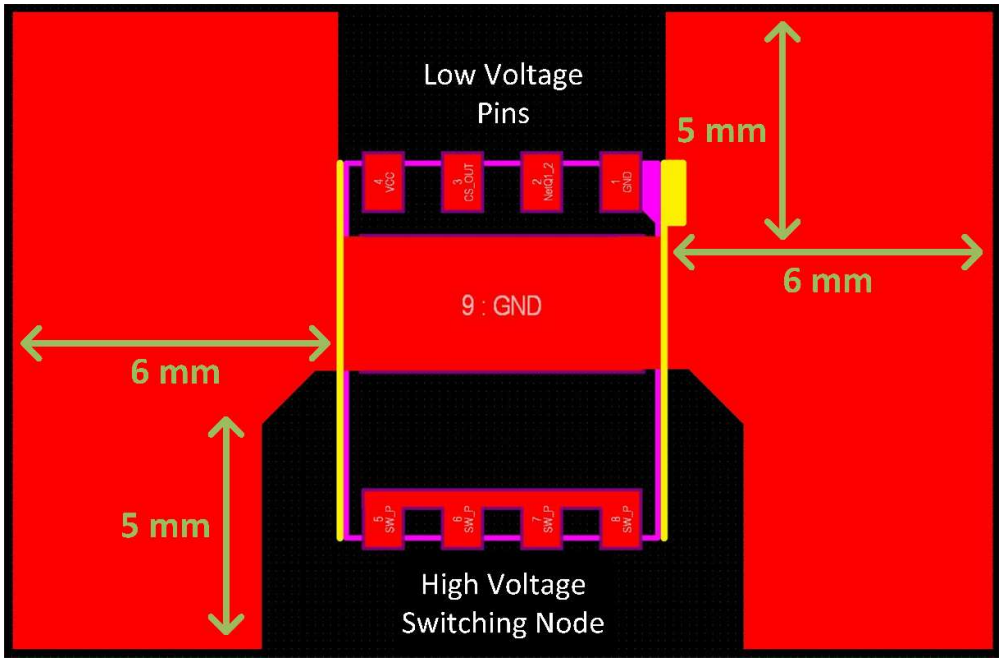

Figure 6 - Recommended Minimum Area Pattern for Same-Side Copper Area on Example DFN5x6

Because the power pad is connected to the source and the source is at ground potential, the pattern of Figure 6 should be expanded as much as possible, coming with no risk of greater radiated nor conducted EMI. This was shown in practice in the QR Flyback Evaluation Board from CGD, where primary ground occupies most of the component and opposite sides of the PCB.

MAKING THE MOST OF THE OTHER PCB LAYERS

It is not always possible to incorporate enough copper area on the component side of the PCB. Designs with two or more copper layers should use arrays of thermal vias to connect copper areas on different layers. Thermal resistance to opposite side copper, and internal layer copper pours or planes, decreases with the number of thermal vias that are perpendicular to the sources of heat (the source pad of ICeGaN™). Performance improvement with increased via count drops off quickly as the vias get further from the source pad (the heat source). The optimum solution is to fill the area directly under the exposed pad with an array of vias. [4] [5] The plated barrels of the vias are essentially small copper tubes that serve as conduits for heat to the opposite side and/or internal PCB layers.

THERMAL VIAS VS MANUFACTURABILITY

Thermal management and manufacturability may conflict. Vias with holes that are too large can wick solder away from the exposed pad via capillary action. Vias that are too small increase manufacturing cost (PCB manufacturers will specify a minimum size below which costs increase). As the via diameter reduces, it becomes harder to deposit copper plating evenly along the via barrel. The compromise is to carefully select the via hole size to both minimize solder wicking and maximize the filling of the via barrel with copper. A minimum of 35 µm of copper thickness is recommended for most power supply PCBs, and when the PCB will be used for cooling of SMT packages, 70 µm provides a significant improvement when the budget allows. [4] Arrays of vias with 0.25 mm holes (before

plating) and outer diameters of 0.5 mm spaced 0.75 or 0.8 mm apart, on both the X and Y axis, are a good compromise between heat transfer and manufacturability. In practice, it is difficult to achieve 70 µm plating on the inside of vias with such small holes with good repeatability. However, 35 µm of copper thickness still fills in a significant portion of the via barrel with copper, reducing the probability of solder wicking.

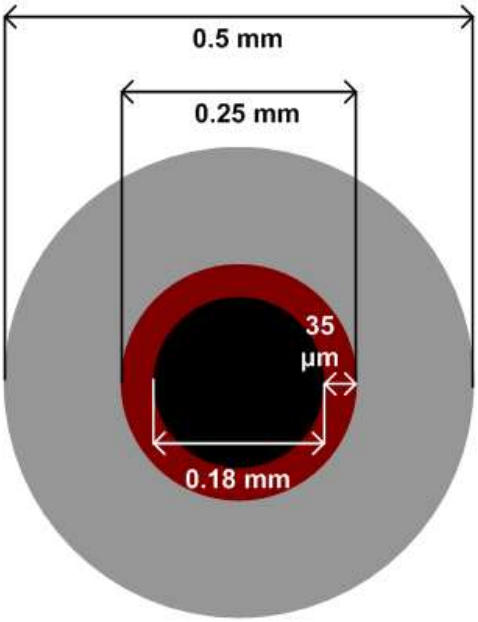

Figure 7 - Detail of Recommended Thermal Via, to Scale, Showing Thickness of 35 µm Copper Plating

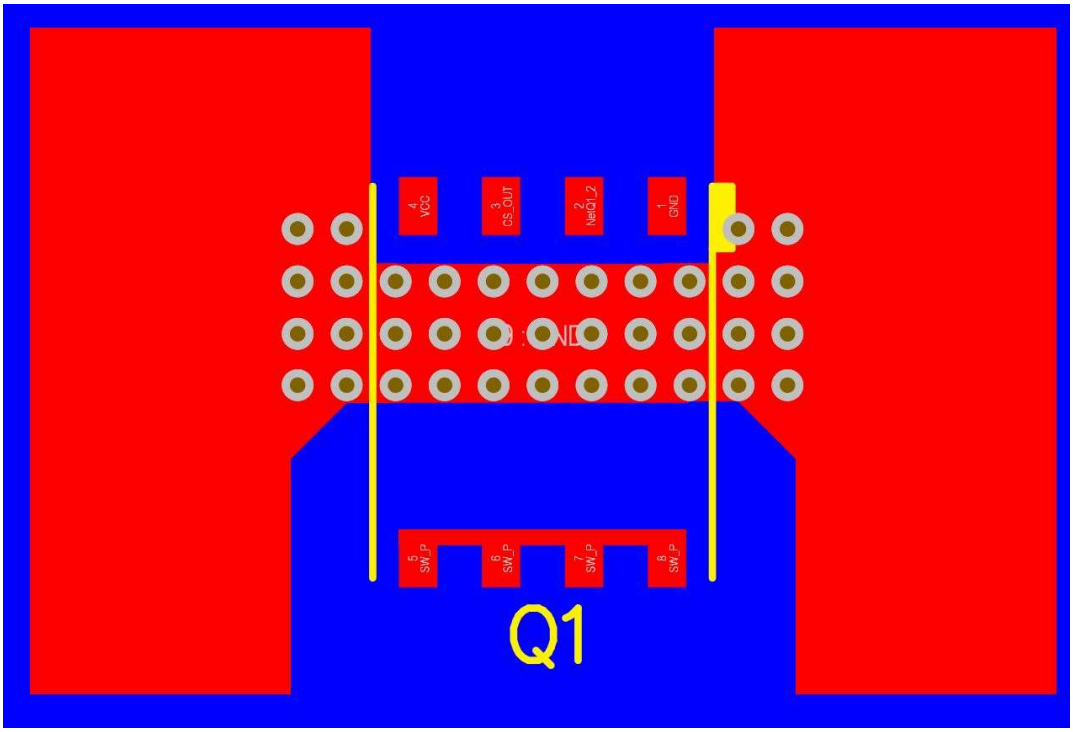

Figure 8 - Recommended Thermal Via Array Within Source Pad on an Example DFN5x6

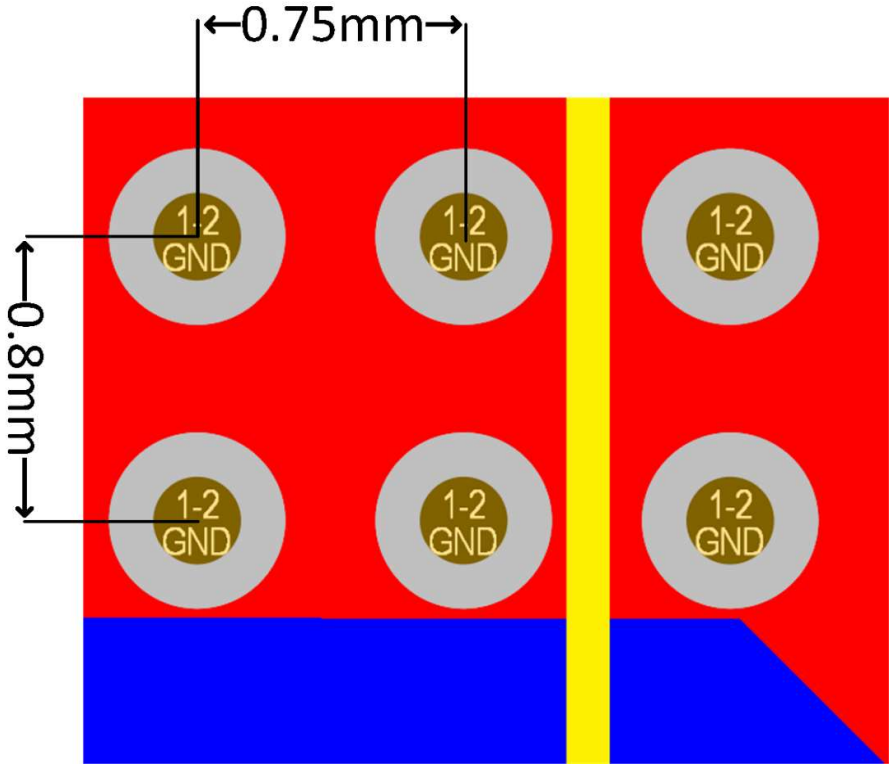

Figure 9 Close Up Image of Example Via Spacing

VIA TENTING

Tenting is the process of covering a via hole with solder mask. It can be applied to the component side or the opposite side. Tenting both sides is rarely done because it traps air in the barrel that expands due to heat during assembly and can deform the PCB surface. Tenting on the component side of the PCB (underneath the HEMT) is generally preferred because it stops solder from flowing into the vias, however it does reduce the contact area between the thermal pad and the PCB. Tenting on the opposite side of the PCB has a perceived disadvantage due to outgassing from the solder flux that can cause voids. [4]

An alternative technique, called encroaching, allows some solder wicking but limits the volume of solder drawn to the opposite side of the PCB by leaving small annular rings of exposed copper around each thermal via on the opposite side. If performed properly this can help fill the via barrels with solder for a slight improvement in thermal resistance. However, the technique causes small bumps that make surface mount heatsinks impractical on the opposite side.

CGD does not make a recommendation on either tenting or encroaching vias as the benefits between these methods will vary with the final application and the thermal performance differences are minimal.

THERMAL RESISTANCE TESTS

The DFN5x6 package was tested to determine the junction-to-case thermal resistance (Θ_{JC}) for the source thermal pad. Results were from 1.41 to 1.53 °C/W. One created a single-sided test PCB with a component side copper shape connected to the source of around 100 mm^2 and another copper

shape of around 300 mm^2 connected to the drain pins. For a power dissipation of 2.3 W this configuration gave a junction-to-ambient thermal resistance Θ_{JA} of around 50 °C/W.

To obtain Θ_{JA} data with a precisely defined power dissipation on a two-layer PCB, a test fixture was developed to operate an ICeGaN™ HEMT in the DFN5x6 package as the pass element of a linear regulator. This allowed the power dissipation to be tightly controlled by setting the variables in the power dissipation equation for linear regulators.

$$P_{DISS} = (V_{IN} - V_O)I_O \qquad (1)$$

The control loop of the linear regulator controller actively adjusts the on-resistance of the HEMT regardless of temperature. The test fixture itself consists of the ICeGaN™ HEMT on a breakout PCB allowing access to all its pins, and a separate control PCB with the linear regulator controller and associated circuitry. The breakout PCB has 744 mm^2 of 35 µm thickness copper connected to the source pad on its top layer, 1270 mm^2 of 35 µm thickness copper connected to the source pad on its bottom layer and an array of fifty-two 0.5 mm diameter, 0.25 mm hole diameter thermal vias connecting the two layers. A complete schematic and PCB layout for the breakout PCB are given in Appendix B. Table 1 and Table 2 show the results.

Testing was carried out in still air with one thermocouple measuring ambient temperature, a second thermocouple bonded to the top of the HEMT case and the ICeGaN™ junction temperature was measured with a thermal imager. Two measuring methods were used to show correlation between different measurement techniques and ensure the accuracy of the data presented.

These results indicate that an engineer can expect a junction temperature rise of between 30 °C/W and 35 °C/W when using the recommended minimum copper area and vias for thermal relief as described previously.

Input Voltage (V)	Output Voltage (V)	Output Current (A)	Power Dissipation (W)	Ambient Temp (°C)	Case Temp (°C)	Case Temp Rise (°C)	Junction to Ambient Thermal Resistance (°C/W)
4.3	3.3	0.1	0.1	16.5	20.1	3.6	36
4.3	3.3	0.2	0.2	16.7	24.9	8.2	41
4.3	3.3	0.5	0.5	17.0	34.3	17.3	34.6
4.3	3.3	1	1	17.2	49.1	31.9	31.9

Table 1 - Junction-to-Ambient Thermal Resistance of a DFN5x6 ICeGaN HEMT Using Thermal Imaging

Input Voltage (V)	Output Voltage (V)	Output Current (A)	Power Dissipation (W)	Ambient Temp (°C)	Case Temp (°C)	Case Temp Rise (°C)	Case to Ambient Thermal Resistance (°C/W)
4.3	3.3	0.1	0.1	16.1	22.1	6.0	60.0
4.3	3.3	0.5	0.5	16.8	34.1	17.3	34.6
4.3	3.3	1.0	1.0	17.0	47.5	30.5	30.5

Table 2 - Case-to-Ambient Thermal Resistance of a DFN5x6 ICeGaN™ HEMT Using Thermocouple Bonded to Package Top Surface

Conclusion

Overall, thermal management for ICeGaN in either package can be summed up as follows, listed in order of importance:

- Use a H/dog bone shape on the component side to maximize copper area while respecting the creepage and clearance limits.
- Fill the entire source pad with an array of thermal vias.
- Extend the opposite side copper as much as possible in all directions except towards the drain connection. Do the same for any internal layers if they are available.

Regarding the best practice for electrical design:

- Keep the drain of the HEMT as close as possible to the pin(s) or pad(s) of the switching inductor or transformer winding in order to minimize the switching node area.
    - In the case of a high-side HEMT (for example, buck converter or top transistor of a half-bridge) it is the source that must be kept close the inductor/transformer connection.
- Use a solid shape that is just enough to cover the ICeGaN drain pads (5-8) and the inductor/transformer pins/pads, again to minimize switch node area.
- Do not run GND or any other nets on the opposite or internal layers underneath the switching node. Instead, place areas of identical shape and size on the other layers and connect with vias. This maximises total copper area for heat sinking.
    - Use 0.5 mm diameter, 0.25 mm hole vias used for thermal management are effective at stitching the switch node shapes together.

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Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	JF	18/03/2022

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