ICeGaN™ DHDFN package

Overview

This document describes the dual-side cooled DHDFN 10 x 10 mm^2 SMD package which accommodates the new 25 mΩ and 55 mΩ ICeGaN P2 series.

ICeGaN devices are CGD's easy-to-use 650-V GaN-HEMT devices, which can be driven like a MOSFET.

CGD's ICeGaN gate technology offers a high gate threshold, broad gate voltage window, and exceptional gate robustness. DHDFN package has been designed for thermal optimisation, this package features a thermally-enhanced high-power design and a compact 10 x 10 mm^2 PCB footprint.

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Nomenclature

CS	Current sense
dc	Direct Current
DHDFN	Dual heat-spreader dual flat no leads
I_{DS}	Drain-source current
KS	Kelvin source connection
NC	No connected
PCB	Printed circuit board
PFC	Power factor correction
R_{thJC}	Junction to case thermal resistance
R_{thJH}	Junction to heatsink thermal resistance
$R_{thSOLDER}$	Solder thermal resistance
R_{thPCB}	PCB copper vias thermal resistance
R_{thTIM}	Thermal interface thermal resistance
SMD	Surface mount device
T_{amb}	Ambient temperature
T_C	Device case temperature
T_J	Device junction temperature
TPPFC	Totem-pole power factor corrector
TIM	Thermal interface material
TOLT	TO-leaded top-side
UPS	Uninterruptible power supply
V_{DD}	Low-voltage supply to ICeGaN circuitry
V_{GS}	Gate–source voltage
$V_{GS(th)}$	Gate–source threshold voltage

1 Introduction

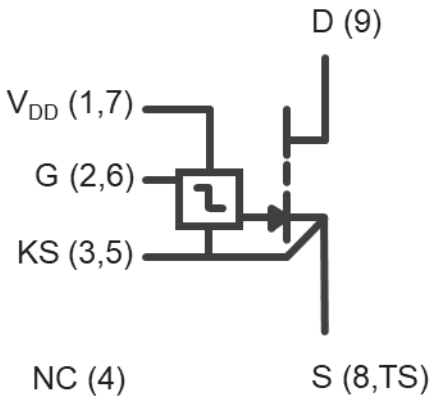
The DHDFN package represents a significant advancement in power device packaging technology. Engineered to optimise thermal dissipation and layout flexibility, the DHDFN package offers unique advantages for high-performance power electronics applications.
DHDFN package features dual-side cooling, allowing heat to dissipate from both the top and bottom of the device. This innovative design significantly enhances thermal management capabilities compared to traditional packages, which typically dissipate heat from only one side. Another notable feature of the DHDFN package is its dual gate design, which provides additional flexibility in layout and aids thermal performance optimisation.

In this application note, our focus will be on the DHDFN package housing the CGD65D025SP2 ICeGaN™ (650 V, 25 mΩ, P2 series). ICeGaN devices are 650-V GaN-HEMT which can be driven like a MOSFET with a standard driver IC. For more information about ICeGaN technology, how to drive it and its advantages, refer to references [1] and [2]

2 DHDFN-9-1 features

2.1 Terminal package structure

Figure 1 depicts the ICeGaN symbol, pin out and the external view of the DHDFN package.

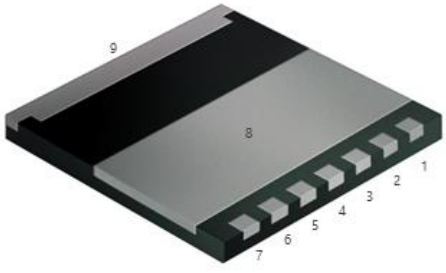


(a)

(b)

Pin number	Name
1, 7	VDD
2, 6	Gate
3, 5	Kelvin Source
4	No Connected
8	Source
9	Drain
TS	Top side heat spreader

(c)



(d)

Figure 1 – (a) ICeGaN symbol (b) DHDFN top view and pin out (c) ICeGaN pin-out (d) DHDFN bottom view and pin out

ICeGaN in DHDFN package is a 6-terminal / 9-pin device with an additional top side thermal pad: Drain (D), source terminal separated into Kelvin Source (KS) and Source (S), also connected to the thermal pad (TS), VDD pin; pin 4 is not connected. The Gate (G), VDD and the Kelvin Source (KS) terminals have two pins arranged symmetrically around the pin 4 (NC) on the side of the package. The KS terminal is utilised for the return of the gate signal. The VDD must be supplied with a 9 V to 20 V dc voltage for the correct ICeGaN operation. The top-side thermal pad (TS) was designed to accommodate a heatsink.

2.2 Dimensions

DHDFN is a 10 mm x 10 mm x 0.635 mm surface-mounted package comparable to TOLT, designed for high-power applications where efficiency and power density are top priorities. Figure 2 shows the dimensions of the DHDFN package.

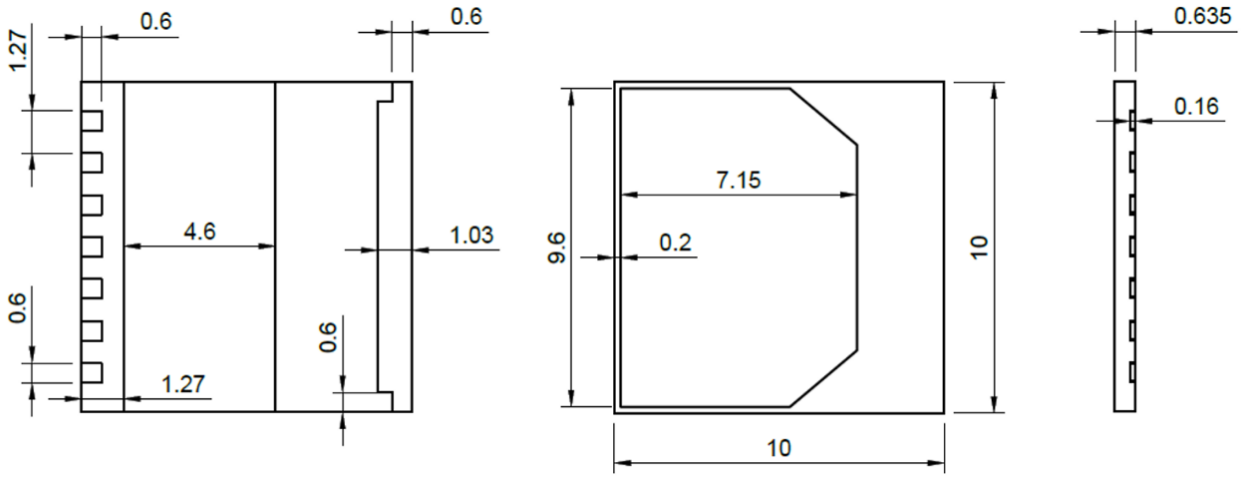


Figure 2 – DHDFN package dimensions in millimetres (mm)

DHDFN incorporates an ample top-side thermal pad plus a large source-pin thermal pad connection with an area of approximately 46 mm^2.
The DHDFN package features a 3 mm creepage between the source and drain pins, which exceeds the 2.795 mm gap found in the through-hole TO-247 package. ICeGaN not only can be considered as a discrete-GaN surface-mounted package replacement but also as an alternative to SiC technology in many applications, with the DHDFN package being an optimal alternative to the through-hole TO-247 package.

3 Layout considerations

3.1 Footprint

Figure 3, illustrates the recommended DHDFN footprint.

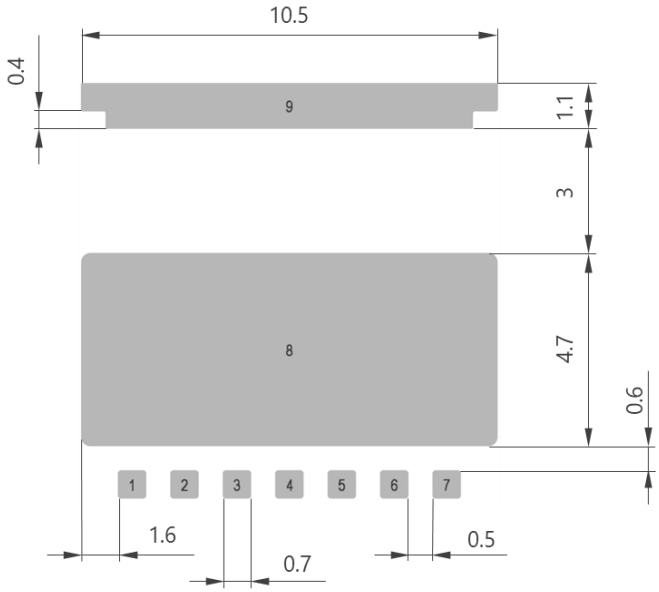


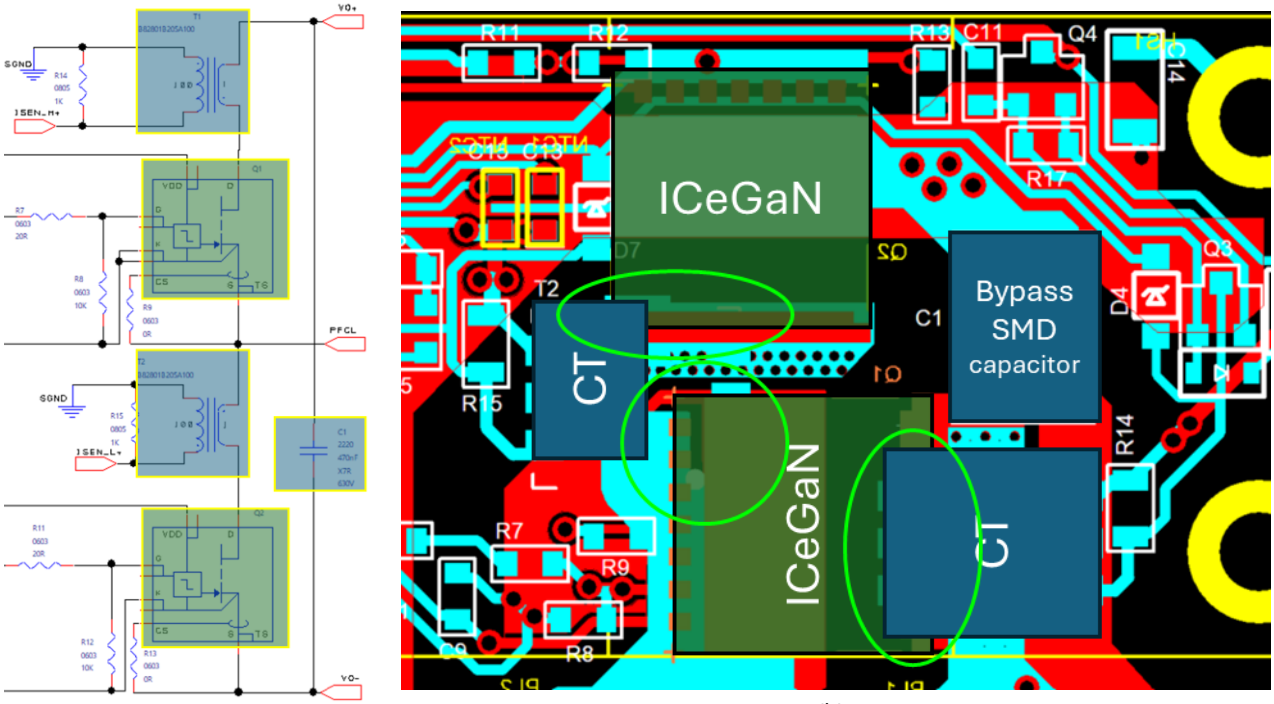
Figure 3 DHDFN footprint (figures in mm)

The PCB copper on the source pad can be used to add copper vias beneath the device to transfer the heat to a heatsink on the other side of the PCB for dual-heatsink arrangement.

3.2 Layout example: top-side cooled layout in half-bride configuration

The DHDFN package enables compact and efficient layout designs, particularly in half-bridge configurations. By leveraging the top-side cooling capability, engineers can optimise power loop layouts for minimal parasitic elements and improved thermal performance.

One of the DHDFN package's layout advantages is the placement of components, for example dc bypass capacitors, directly underneath the two DHDFN packages. This configuration creates a tight power loop, maximising efficiency and minimising parasitic effects. Such a layout is not feasible with bottom-cooled packages utilising vias for heat dissipation. Figure 4 illustrates an example where current transformers in series with each ICeGaN devices are placed underneath the DHDFN package, reducing the power loop. In this example the high side (HS) ICeGaN is rotated by 90 degrees anti-clockwise to have the shortest path between the LS drain and the HS source terminals

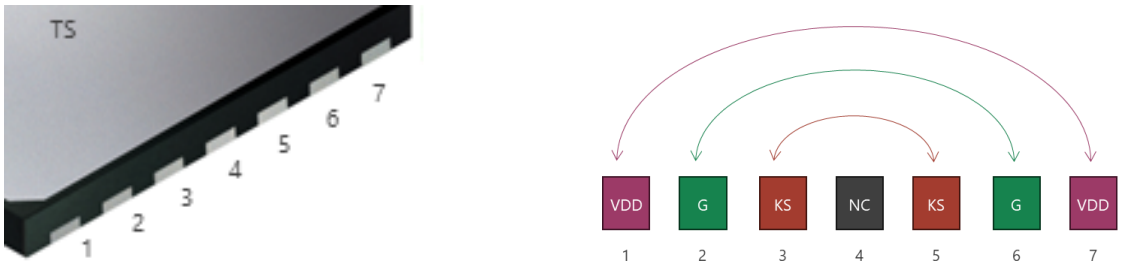


(a) (b)

Figure 4 – Half-bridge layout example. (a) Half-bridge schematic (b) Half-bridge placement

3.3 Layout Example: dual gate for single device use and paralleling

Engineers can leverage the dual-pin feature for the Gate, VDD and Kelvin source terminals of the DHDFN package for both a single device and paralleling applications. The symmetrical dual pin-out is illustrated in Figure 5



(a) (b)

Figure 5 - Symmetrical dual pin-out terminals

For single device half-bridge applications, only one pin for each terminal will be utilised, while the other pin can remain floating. The option to choose one pin or another simplifies layout design.

When paralleling multiple devices, the symmetrical dual pin-out feeding the gate drive signal in the middle facilitates symmetric layout implementation, illustrated in Figure 6 and Figure 7. This ensures balanced operation and maximises overall system efficiency. Ther outer pins of each device can be left floating. In the example corresponding to the figures mentioned, these pins are used to add test points without interfering with the gate loop.

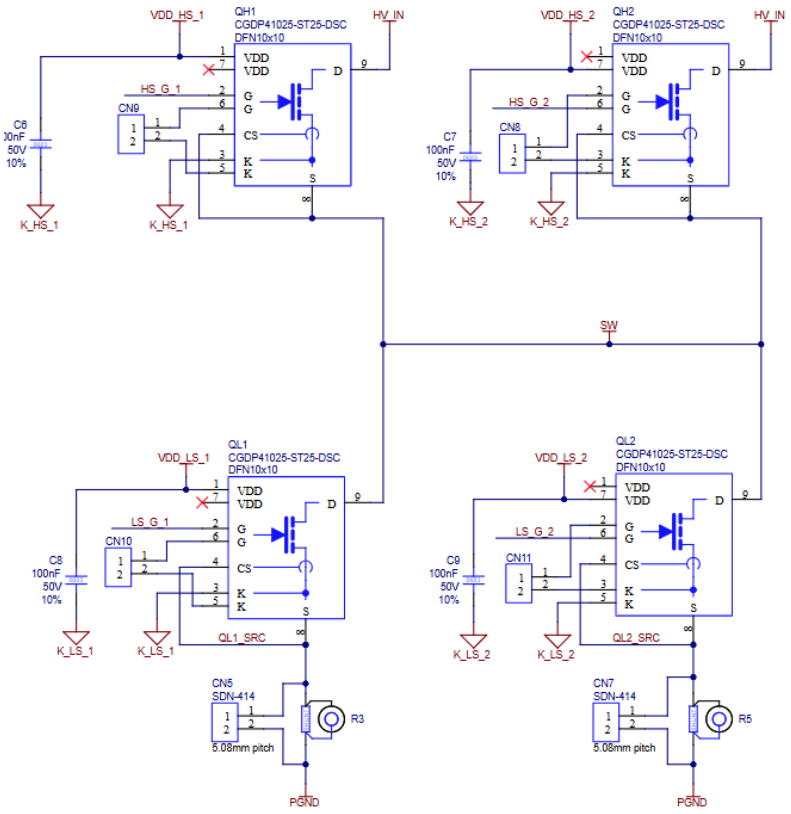
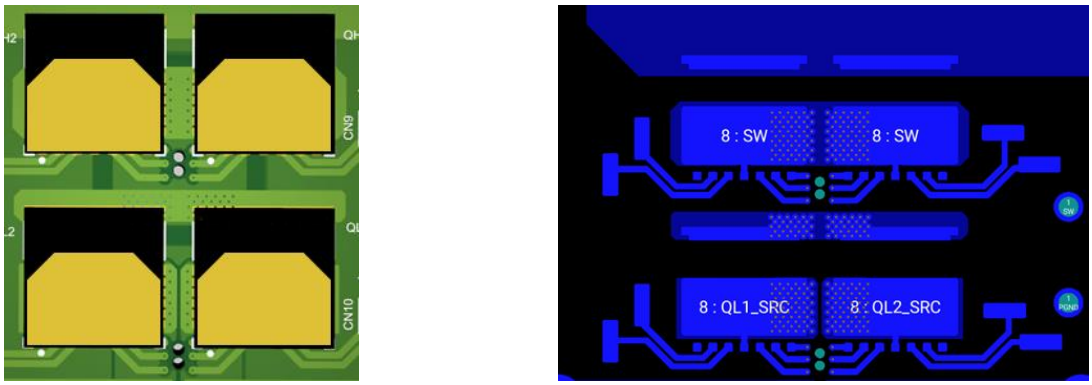


Figure 6 - Half-bridge schematics with paralleled ICeGaN



(a) (b)

Figure 7 - Half-bridge layout example with two DHDFN ICeGaNs in parallel

4 Heatsink guidelines

4.1 Top-side heatsink configuration

DHDFN package offers the possibility of either top-side cooling or dual-side cooling. The DHDFN package can also be used in bottom-cooled only configuration, although for such applications we recommend CGD's BHDFN package.

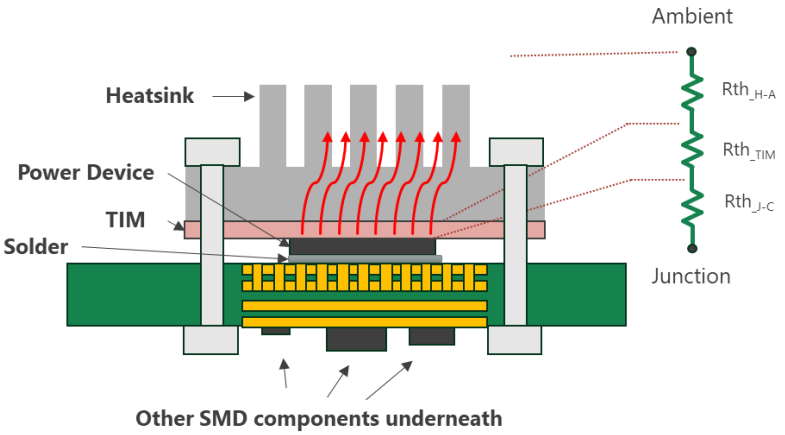


Figure 8 – Top-side cooling heatsink assembly

Top-side cooling offers a straightforward solution for dissipating heat from the DHDFN package, ensuring efficient thermal management and having the possibility of using the space underneath the PCB to place other components which can result in compact designs in a wide range of applications.

Figure 8 illustrates the heatsink assembly with top side cooling; In this particular representation shows how the vias don't cross the full PCB stack, and in a 4-layer board like this, the first 2 layers can be used for the power path, the third layer could well be the 0-volts reference plane and the bottom layer is used to allocate any other SMD components underneath the ICeGaN. The thermal pad on the top is directly connected to a heatsink through a TIM. Unlike bottom side cooled packages, the heat does not travel through the PCB and copper vias which increases R_{thJA}. The total thermal resistance from the junction to the ambient environment comprises only three components:

- The thermal resistance from the junction to the package case (R_{thJC}), which is determined by the design of the package.
- The thermal resistance of the thermal insulating material that is used between the device and the heat sink (R_{thTIM}).
- The thermal resistance of the heat sink from the thermal insulating material to the surrounding environment (R_{thHA}).

Below there is an example of top-side cooling; Figure 9 shows the front of a TPPFC half-bridge board in which all the driving and current sense components are visible and Figure 10 shows the back of the same board, featuring the heatsink.

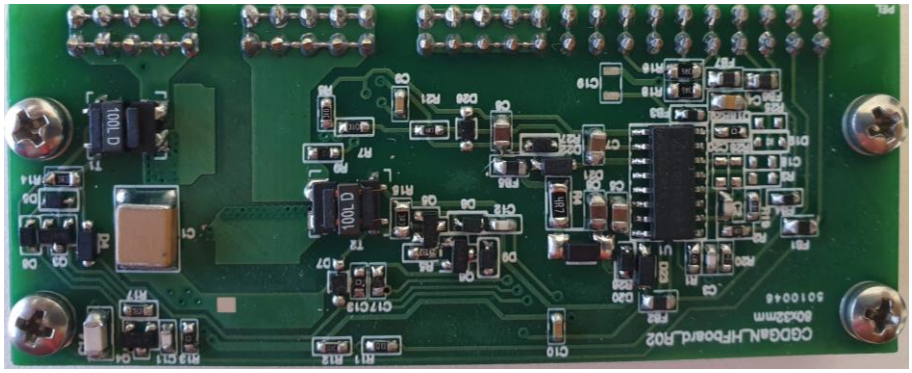


Figure 9- Top-side cooling example: SMD component side

Figure 10 - Bottom-side cooling example: heatsink side

4.2 Dual-side heatsink configuration

For applications requiring enhanced thermal dissipation, a dual-side cooled two-heatsink solution can be implemented. This configuration maximises heat transfer from both sides of the package, effectively reducing the junction temperature. Reducing T_J means reducing $R_{DS(on)}$ increase due to temperature increase. This helps to increase the overall efficiency of the system.

The dual-side cooling technique, while effective for heat dissipation, limits the available space for placing other components underneath the ICeGaN in DHDFN. This is due to the heatsink, which is utilised for the cooling process, occupying that space. However, the benefit is that it allows for better thermal management, which can enhance ICeGaN's thermal performance. There is always a trade-off between thermal performance and space in such designs.

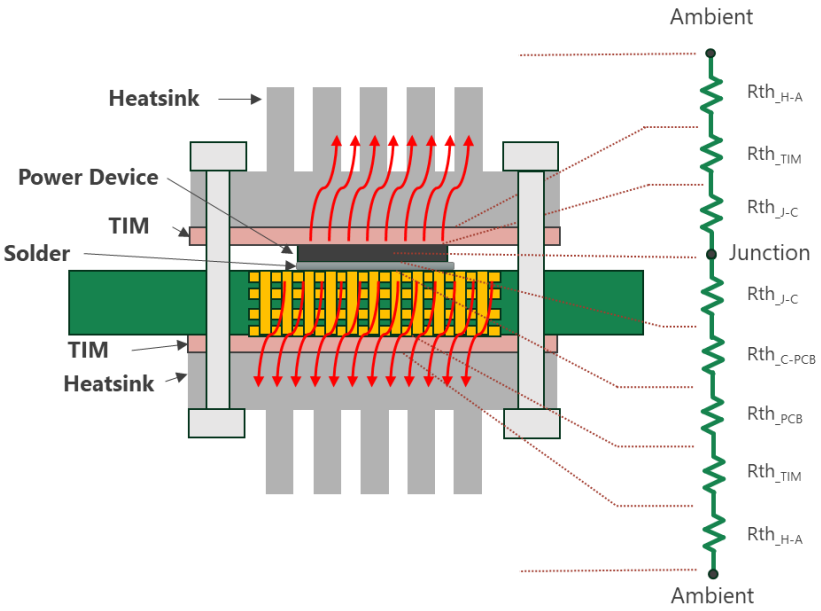


Figure 11 – Dual-side cooling heatsink assembly

Figure 11illustrates the two heatsink connections to have effectively two R_{thJA} in parallel. As mentioned in section 1.1 the R_{thJA} will be lower for the top side.

4.3 TIM recommendations

The top side of the DHDFN package is electrically connected to the ICeGaN source terminal. The function of this thermal insulating material is to ensure optimal contact between the surface of the device and the heatsink, and to provide electrical insulation between the die/package and the heatsink.

To reduce thermal resistance to a minimum, it is key to ensure that the two surfaces of the device and the heatsink are in best possible contact, and the TIM selected has a low thermal resistance.

4.4 Heatsink mounting recommendations

Heatsink design and mounting techniques and TIM are crucial for optimising thermal performance and reliability. Predominantly, high-power application topologies utilise half-bridge configurations which means the pair of ICeGaNs must be connected to a heatsink. The easiest way to create contact of these devices mounted on the PCB with the heatsink is to use screws. This technique could potentially create stress on the PCB, resulting in its deformation and resulting in poor mechanical contact.

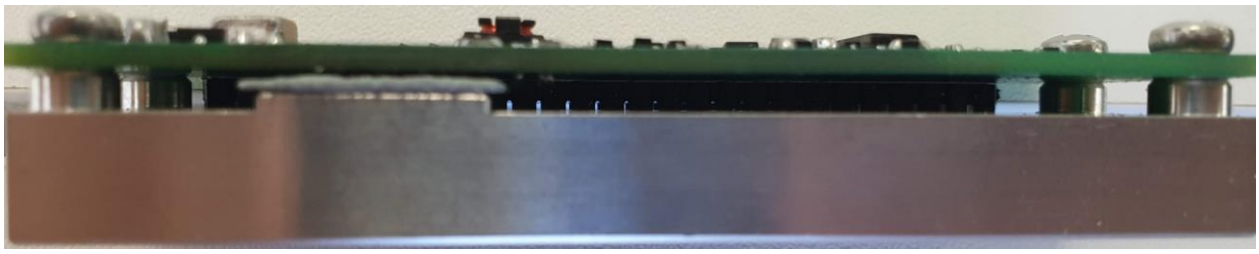


Figure 12 – Top-side cooling heatsink mounted on a PCB

Figure 12 shows an example of a top-side heatsink assembly for two ICeGaNs in a half-bridge configuration. The half-bridge layout has been optimised to have a small power loop, see Figure 4, The heatsink is mounted with four M4 screws

using spacers, and the it is customised with a “step” . This step or hump, zoomed in Figure 13, was designed with enough area to cover the thermal pads of both ICeGaNs. This design allows a good thermal contact with only minimal torque to the screws to avoid bending of the PCB.

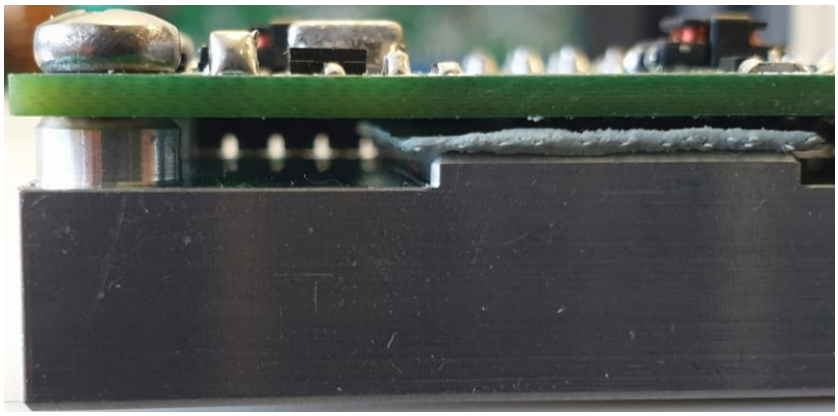


Figure 13 – Details of the top-side cooling heatsink designed to improve mechanical contact

5 Thermal simulations

Thermal simulations were conducted to compare the thermal performance of CGD’s dual-side cooled (DHDFN) package against CGD’s bottom-side cooled (BHDFN) package and also TOLT package that is becoming commonly used by GaN competitors. All simulations were done in Ansys, where the abovementioned 3 packages were placed on a JEDEC-standard PCB.

5.1 Thermal simulation environment and assumptions

To conduct a fair comparison of the thermal performance of the different packages, everything apart from the package itself was kept constant as much as possible. That is, the heatsinks, and TIMs were identical, and so was the GaN die housed within the package. There were minor differences between the PCBs to account for the differences in the footprint of the 3 packages.

For the purpose of this study, it was assumed that CGD’s 25 mΩ die was housed in each package. The active and passive volumes were considered to be pure GaN and none of the circuits and wires within this layer were modelled. It was assumed that power was dissipated uniformly across the active region. The temperature-dependence of this parameter was not given and therefore this was assumed to be constant in the simulations. The outer surface of the heatsink was set to a temperature of 50 °C. The value of this set temperature does not affect the extracted value of R_{thJH}. All other boundaries were kept insulated, and there was no heat exchange with the atmosphere.

The die was attached to the copper lead frame using a ‘die attach’ material The thermal conductivity of this material was assumed to be 8 W/m·K.

The simulation results are useful in providing comparison between the packages. However, the absolute measured value of R_{th} depends on the precise thermal conductivity/resistance-values of contributing materials including the solder joints, interconnects and die-attach. The thermal conductivity of several of these is not known accurately, and approximate and/or temperature-independent values were used instead.

5.2 DHDFN vs BHDFN vs TOLT

Table 1, Table 2 and Figure 14 summarise the results of the simulations.

Thermal simulations have confirmed our expectations: the DHDFN package with dual-side cooling offers the most efficient thermal resistance (R_{thJA}), making it the optimal choice for cooling ICeGaN in high-demand power systems. When compared to the BHDFN with a bottom-side heatsink, the DHDFN with top-side cooling provides significantly lower R_{thJA}. Nevertheless, it is fair to say there's room for performance enhancement in the BHDFN by optimising the via arrangement on the PCB.

The simulation results show that DHDFN package has a lower R_{thJA} than the TOLT package which has the exact same die inside. DHDFN thermal pad area is bigger than that of TOLT. For instance, under 20-W dissipation, the DHDFN package would run approximately 14 °C cooler than a TOLT package.

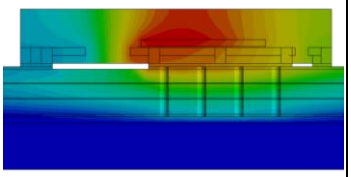
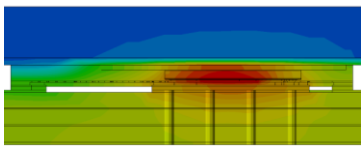
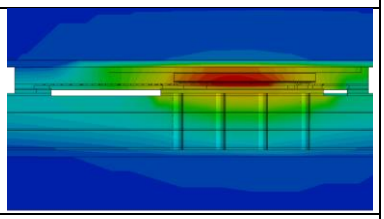
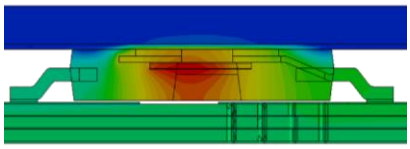
	Bottom-side heatsink (°C/W)	Top-side heatsink (°C/W)	Dual -ide heatsink (°C/W)
BHDFN		-	-
DHDFN	-		
TOLT	-		-

Table 1 – Thermal images of all simulations

Geometry	Bottom-side heatsink (°C/W)	Top-side heatsink (°C/W)	Dual-side heatsink (°C/W)
BHDFN	4.0	-	-
DHDFN	-	1.9	1.5
TOLT	-	2.6	-

Table 2 – Simulations of R_{thJA} values of DHDFN, BHDFN and TOLT packages with 25mΩ die

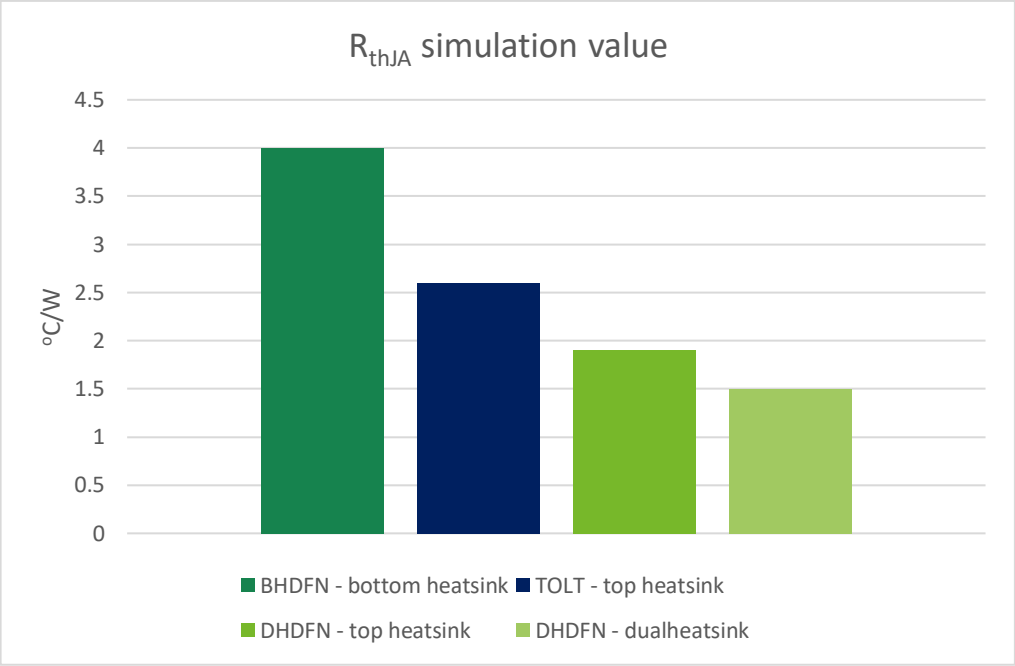


Figure 14 - R_{thJA} comparison

6 Conclusion

CGD's DHDFN package presents a significant enhancement in thermal management for high-power applications, offering the flexibility of both top-side and dual-side cooling configurations. This versatility allows for efficient heat dissipation, effectively reducing the junction temperature and enhancing the overall system performance. The top-side cooling option provides a straightforward solution for heat transfer avoiding the heat to travel through the PCB and copper vias, resulting in lower thermal resistance. In addition, DHDFN package used with top-side cooling allows for the placement of other components, such as bypassing HV capacitors, directly underneath the package, , creating a compact and efficient design. This configuration is particularly beneficial in half-bridge configurations, where it creates a tight power loop that maximises efficiency and minimises parasitic effects.

For applications requiring enhanced thermal dissipation, a dual-side cooling solution can be implemented, maximising heat transfer from both sides of the package simultaneously.

Furthermore, the DHDFN package features a unique dual-gate pin-out that provides flexibility for PCB design and allows for symmetrical gate loop layout and easier paralleling of ICeGaN.

Thermal simulations show that the DHDFN package outperforms the more traditional TOLT package in both top-side and especially in dual-side cooling configurations.

7 References

[1] "CGD65A055S2 - GaN Transistor | Cam GaN Devices." Accessed: Jun. 26, 2023. [Online]. Available: https://camgandevices.com/p/product-CGD65A055S2/

[2] "ICeGaN™ - A Novel Technology for Integrated Power GaN," Cambridge GaN Devices, White Paper CGD-WP2201, Mar. 2022.

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Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	CTB	2024-06-07

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