APPLICATION INTERFACE BOARD

User Guide

CGD-UG2201

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Safety Warning

DANGER: Do not touch the board when high voltages are applied. There are exposed locations of high voltage on the board when connected to a power source. Brief contact may result in serious injury or death. Allow all components to fully discharge before handling the board. This evaluation kit is designed for use by qualified, experienced engineers only. Appropriate safety measures must be put in place before use and the board should never be left unattended.

WARNING: Some components may become hot during operation and remain so afterwards. There is no built in electrical or thermal protection. Operating voltages, currents and temperatures should be monitored closely throughout operation to prevent damage to the board.

CAUTION: This product contains parts susceptible to ESD (electrostatic discharge). ESD prevention procedures must be used while handling the board.

Operating Limits and Recommendations

Operating outside this window is not recommended and may cause damage.

Voltage limits

The CGD GaN devices have a recommended maximum operation of 650V.

Heat dissipation

Heatsinking the CGD GaN devices has been provided through bottom side thermal connection to the Application Interface Board (AIB), from top-side to bottom-side of the AIB, then through bottom side thermal connection to the recipient PCB assembly. As a result the thermal stack-up will add contributions $R_{\theta\ TOP\text{-}SOLDER} + R_{\Theta\ AIB\ PCB} + R_{\Theta\ BOT\text{-}SOLDER}$ between $T_{JUNCTION}$ & $T_{AMBIENT}$.

Start up

It is recommended to apply the low voltage VDD input prior to the application of high voltage inputs.

User Guide Overview

This user guide will outline the Application Interface Board (AIB) and detail how the customer can use the AIB in their own designs. It will explain the AIB construction, electrical connections and how to assemble to the recipient PCB assembly. This guide, along with the AIB itself is targeted at experienced engineers with an understanding of power electronics and appropriate handling techniques. It will assume the competence of the engineer to safely operate the design with exposed high voltages.

Target Audience

This guide, along with the board itself, is aimed at experienced engineers and assumes a knowledge of necessary equipment to analyse the performance of the board. It is designed to enable SMPS engineers, Design Engineers and Technicians involved in the development of a system to rapidly assess the performance of CGD ICeGaN™.

Technical Support

CGD is happy to provide expert help with any questions or problems. For support, please contact CGD at techsupport@camgandevices.com.

Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	PC	18/03/2022

Contents

1 Application Interface Board Overview

All MOSFET/HEMTs that have been designed to be mounted to a Printed Circuit Board (PCB) have a footprint & Pin-out that the PCB design must comply with. As many electronic component packages & footprints exist, it is often not possible to remove a MOSFET/HEMT of type 'A' and replace with type 'B', without the need to first redesign the recipient PCB. A process that can drive many months of delay before first use of an alternate device is possible.

An Application Interface Board 'AIB' is an adaptor PCB that maps each pin/signal from a CGD HEMT device on the topside of the PCB, to each corresponding pin/signal of an alternative component footprint on the bottom side of the PCB. Hence a CGD device equipped with a suitable AIB can easily be fitted using normal soldering techniques to a recipient PCB that was originally designed for an alternative MOSFET/HEMT.

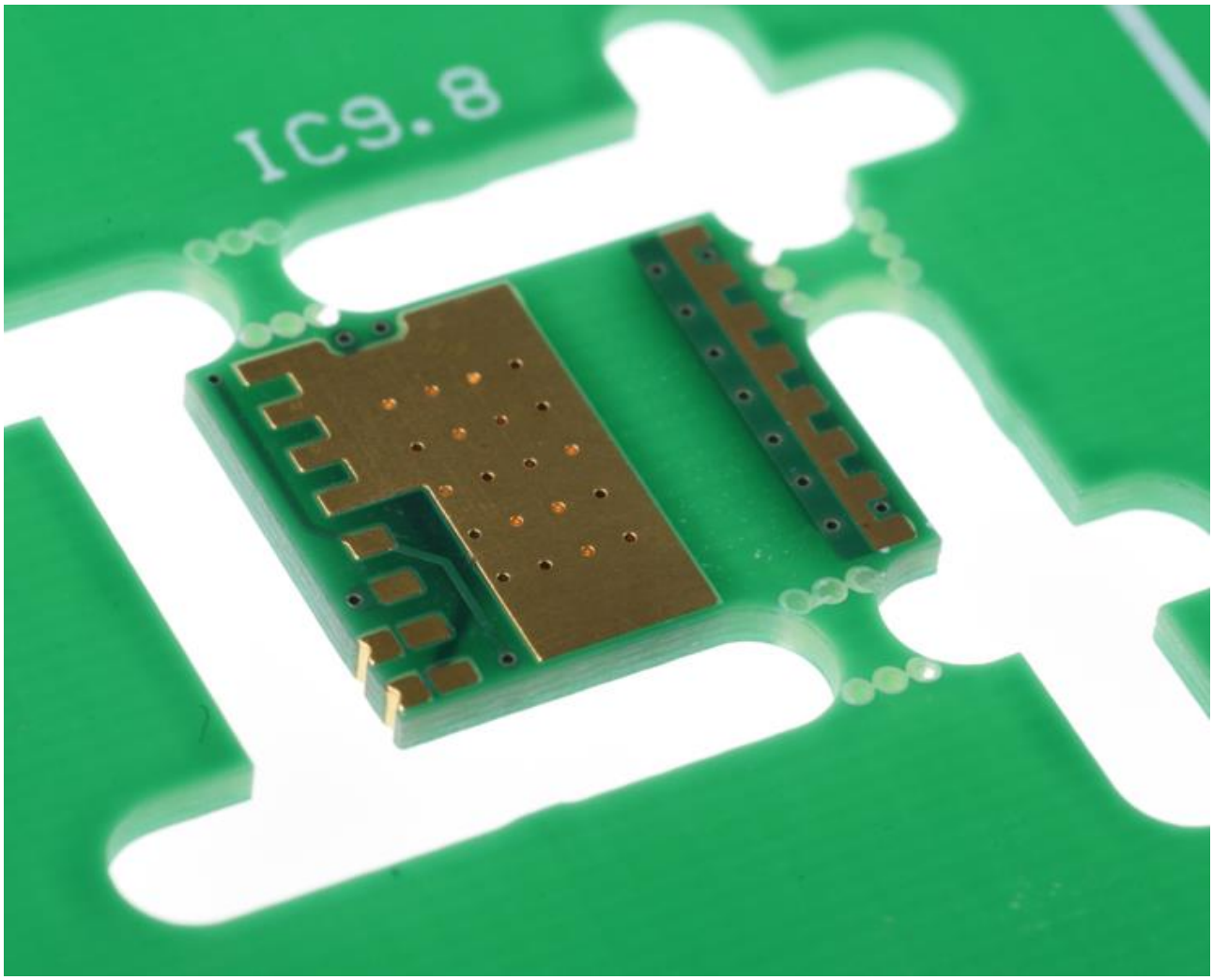


Figure 1 – Bare AIB on PCB Panel

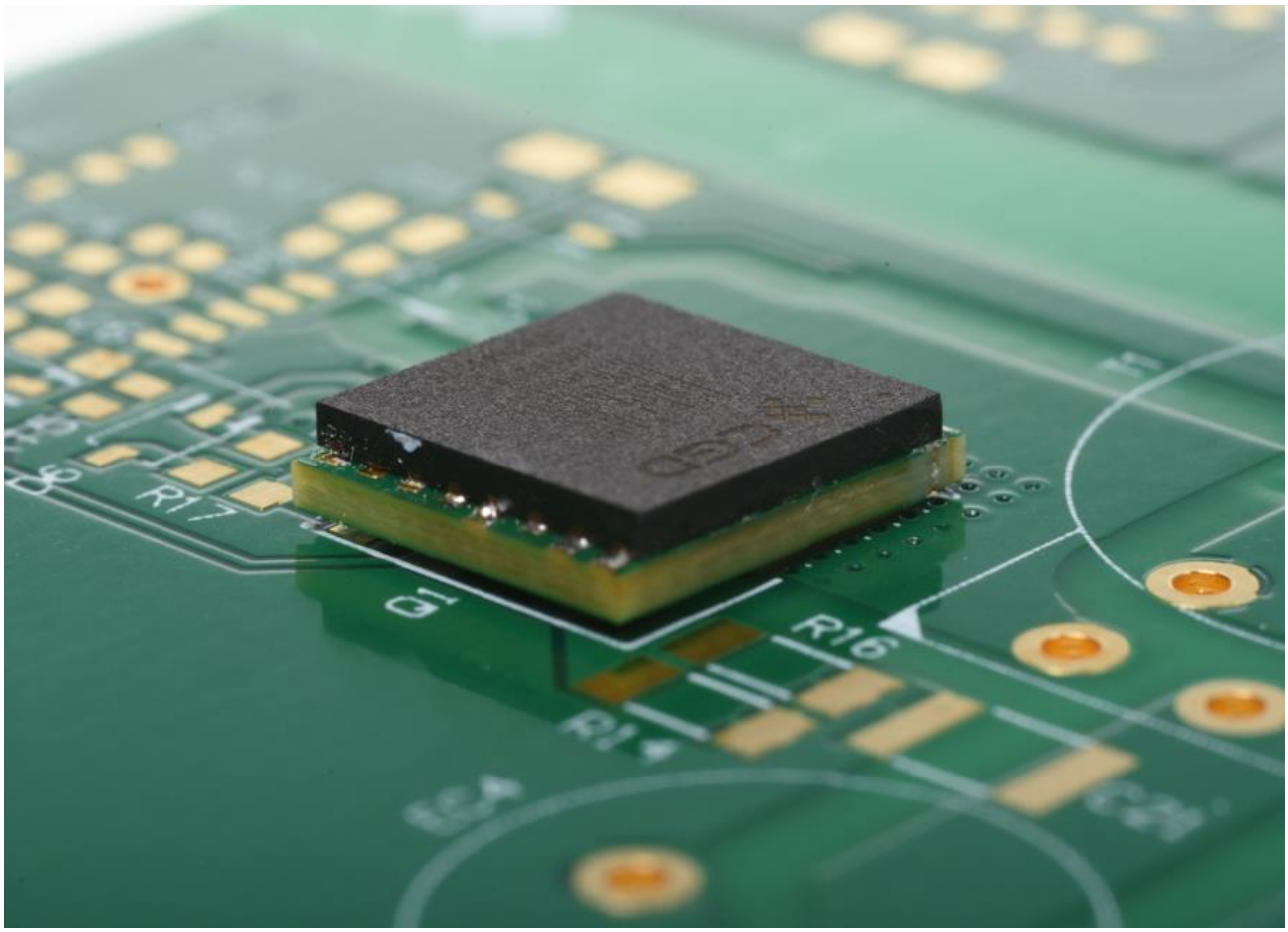


Figure 2 - AIB Mounted to a Recipient PCB Assembly

AIBs are available for all CGD devices and allow their use on recipient PCBs designed around other common PCB footprints/pinouts both SMT & PTH.

The AIB allows 'first assessment' of CGD parts. As the AIB will naturally increase electrical net length and thermal stack-up, the performance will not be optimised and therefore to see the full performance of CGD Devices a PCB redesign will always be required.

1.1 AIB Construction

The AIB PCB is manufactured from FR4 and a 35um multi-layer construction. The top-side footprint will be either CGD DFN5x6 or DFN8x8, bottom-side footprint will be as required to match the recipient PCB design and the internal layers will be designed to map between the two pin-outs while minimising electrical parasitics and thermal resistance.

Figure 3 - CGD DFN 5x6 Package

Figure 4 - CGD DFN 8x8 Package

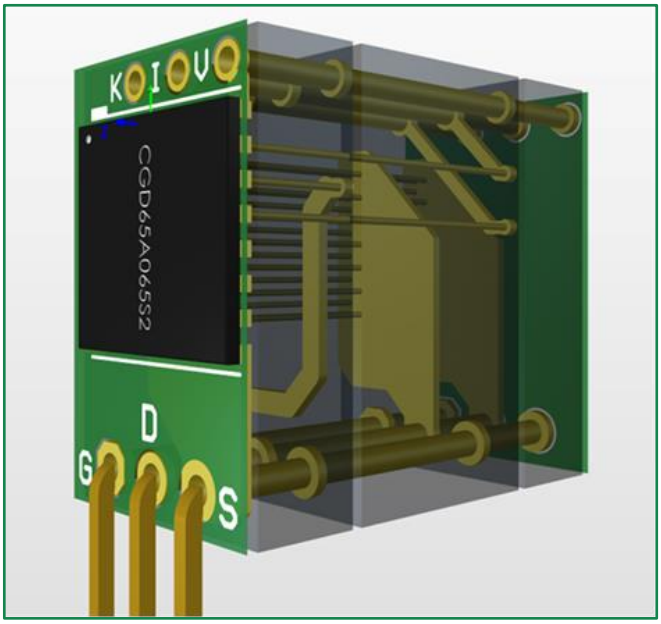


Figure 5 - AIB Construction Showing Internal Layers

1.2 Electrical Connectivity

Typical AIB Electrical Schematic is as shown – actual connectivity will vary dependant on the recipient PCB footprint/pin-out. All AIB variants contain a VDD decoupling capacitor C1.

Some AIB with use V_{DD} signal from the receipt PCB footprint when it is present and in these cases V_{DD} will be provided to the correct ICeGaN™ pin by the AIB. In some cases V_{DD} is not present on the recipient PCB footprint and therefore an alternative V_{DD} source is required from elsewhere on the recipient design.

In all cases refer to the relevant CGD device data sheet to confirm required connectivity and min/max voltage levels - especially for the V_{DD} & CS connections.

Note: It is important that V_{DD} is established prior to application of the device gate signal (turn ON event) – without a valid V_{DD} the ICeGaN™ device will not operate correctly and permanent damage may occur.

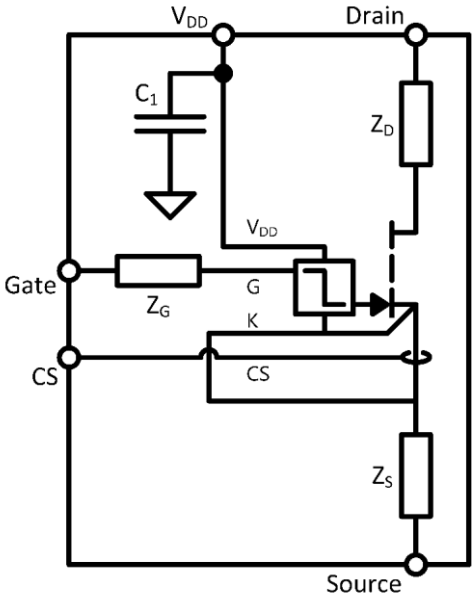


Figure 6 - Typical AIB Electrical Schematic

2 AIB assembly

During AIB assembly to a recipient PCB, precautions should be taken to avoid any excessive heating of the topside CGD device, decoupling capacitor and connections.

Do not use high melting point solder for the assembly of the AIB Assembly to your application circuit.

Do not exceed maximum re-flow limits as stated below and limit local heating to the underside of the AIB PCB.

Parameter	Conditions	Min.	Typ.	Max	Unit
Reflow soldering temperature	T_{reflow}			260	°C

Table 1 - Reflow Parameters for AIB

3 Precautions & Limitations of Use

While every effort has been taken to reduce parasitic effects when using an AIB, the traces used to adapt the CGD device connectivity to the chosen interface footprint will add additional impedances to net lengths.
Dependant on how you wish to use ICeGaN™, especially if operating at the limits of performance care should be taken to gradually increase device power level, monitor switching and ensure waveforms are as expected.

Electrical net lengths are increased when using an AIB

- Gate net length is increased by typically 2-6mm.
- Drain net length is increased by typically 1.6mm.
- Source net length is increased by typically 1.6mm.

Care should be taken to consider the additional net lengths in your design and if necessary, adjust performance as required.

Heatsinking the CGD GaN devices has been provided through bottom side thermal connection to the Application Interface Board (AIB), top-side to bottom-side of the AIB, then through bottom side thermal connection to the recipient PCB assembly. Consequently, the thermal stack-up will add contributions $R_{\theta\ TOP\text{-}SOLDER} + R_{\Theta\ AIB\ PCB} + R_{\Theta\ BOT\text{-}SOLDER}$ between $T_{JUNCTION}$ & $T_{AMBIENT}$. Care should be taken to consider this additional resistance in your design and if necessary, adjust performance as required.

4 AIB Connectivity

This section details the connectivity of each AIB part number, the pin-out between the devices & any additional connections that are required. In all cases the CGD datasheet should be referenced to ensure compatibility with your circuit/design.

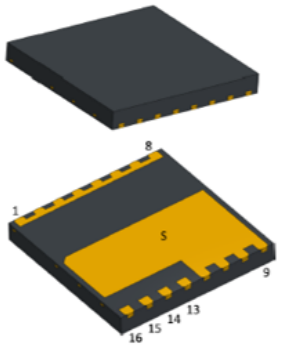
4.1 CGD-ASYINT00101-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

CGD-ASYINT00101-01: GS66508B GaNPX® .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{DD}



CGD65A130S2	GS66508B	Notes
1	1	
2	1	
3	1	
4	1	
5	1	
6	1	
7	1	
8	1	
9	2	
10	2	
11	2	
12	2	
13	4	C1 Pin 1
14	3	
15	NC	Side Castellation
16	NC	C1 Pin 2,Side Castellation

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 7 - CGD-ASYINT00101-01 AIB Pin-Definition

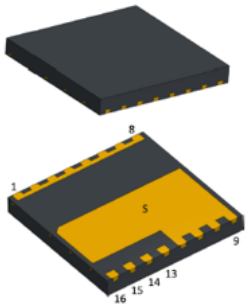
4.2 CGD-ASYINT00201-01 AIB

This AIB does NOT require a separate V_{DD} connection from the customer/recipient PCB.
The AIB/CGD device takes its V_{DD} signal directly from the recipient PCB footprint.

CGD-ASYINT00201-01: NV6115 QFN5x6 .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{ee}



CGD65A130S2	NV6115	Notes
1	5,6,7,8	
2	5,6,7,8	
3	5,6,7,8	
4	5,6,7,8	
5	5,6,7,8	
6	5,6,7,8	
7	5,6,7,8	
8	5,6,7,8	
9	S	
10	S	
11	S	
12	S	
13	NC	C1 Pin 1, Side Castellation
14	2	
15	NC	Side Castellation
16	1	C1 Pin 2

Notes: NC - Not connected
NV6115 - Pins 3,4 are NC
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 8 - CGD-ASYINT00201-01 AIB Pin-Definition

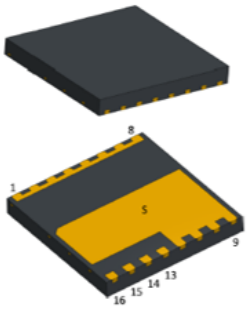
4.3 CGD-ASYINT00301-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

CGD-ASYINT00301-01: GS6530-2L DFN 8x8 .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{ee}



CGD65A130S2	GS6530-2L	Notes
1	5,6,7,8	
2	5,6,7,8	
3	5,6,7,8	
4	5,6,7,8	
5	5,6,7,8	
6	5,6,7,8	
7	5,6,7,8	
8	5,6,7,8	
9	1,2,9	
10	1,2,9	
11	1,2,9	
12	1,2,9	
13	3	C1 Pin2, Side Castellation
14	4	
15	NC	Side Castellation
16	NC	C1 Pin 1, Side Castellation

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 9 - CGD-ASYINT00301-01 AIB Pin-Definition

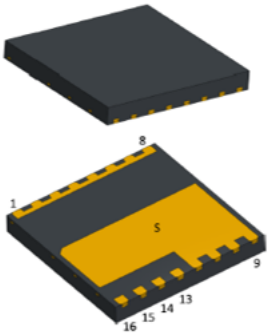
4.4 CGD-ASYINT00401-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

CGD-ASYINT00401-01: IPP60R099P7 TO220 .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{ee}



CGD65A130S2	IPP60R099P7	Notes
1	2, Tab	
2	2, Tab	
3	2, Tab	
4	2, Tab	
5	2, Tab	
6	2, Tab	
7	2, Tab	
8	2, Tab	
9	3	C1 Pin1
10	3	
11	3	
12	3	
13	NC	PTH
14	1	
15	NC	PTH
16	NC	C1 Pin2 & PTH

Notes: C1 - 4.7uF 50V X7R 0603 MLCC
PTH - Plated Through Hole
NC - Not connected

Figure 10 - CGD-ASYINT00401-01 AIB Pin-Definition

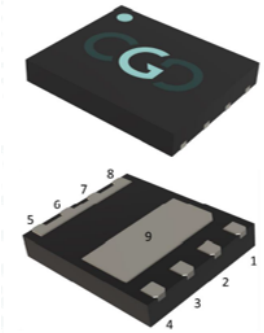
4.5 CGD-ASYINT00501-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

CGD-ASYINT00501-01: IPP60R099P7 TO220 .. To .. CGD65A200S2 DFN5x6

Packaging
DFN5x6 mm

1	Kelvin
2	Gate
3	Current Sense
4	V_{dd}
5-8	Drain
9	Source



CGD65B200S2	IPP60R099P7	Notes
1	NC	PTH
2	1	
3	NC	PTH
4	NC	C1 Pin2 & PTH
5	2, Tab	
6	2, Tab	
7	2, Tab	
8	2, Tab	
9	3	C1 Pin1

Notes: C1 - 4.7uF 50V X7R 0603 MLCC
PTH - Plated Through Hole
NC - Not connected

Figure 11 - CGD-ASYINT00501-01 AIB Pin-Definition

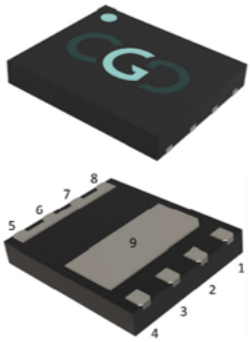
4.6 CGD-ASYINT00601-01 AIB

This AIB does NOT require a separate V_{DD} connection from the customer/recipient PCB.
The AIB/CGD device takes its V_{DD} signal directly from the recipient PCB footprint.

CGD-ASYINT00601-01: NV6115 QFN5x6 .. To .. CGD65B200S2 DFN5x6

Packaging
DFN5x6 mm

1	Kelvin
2	Gate
3	Current Sense
4	V_{dd}
5-8	Drain
9	Source



CGD65B200S2	NV6115	Notes
1	NC	C1 Pin 1
2	2	
3	NC	
4	1	C1 Pin 2
5	5,6,7,8	
6	5,6,7,8	
7	5,6,7,8	
8	5,6,7,8	
9	S	

Notes: NC - Not connected
NV6115 - Pins 3,4 are NC
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 12 - CGD-ASYINT00601-01 AIB Pin-Definition

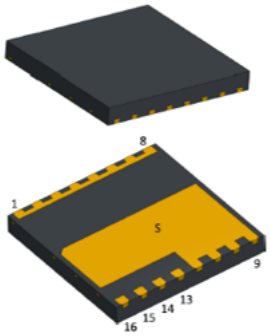
4.7 CGD-ASYINT00701-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

CGD-ASYINT00701-01: IPL60R065P7 ThinkPAK8x8 .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{ee}



CGD65A130S2	IPL60R065P7	Notes
1	5	
2	5	
3	5	
4	5	
5	5	
6	5	
7	5	
8	5	
9	3,4	Side Castellation
10	3,4	
11	3,4	
12	3,4	
13	2	C1 Pin 1
14	1	
15	NC	Side Castellation
16	NC	C1 Pin 2, Side Castellation

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 13 - CGD-ASYINT00701-01 AIB Pin-Definition

4.8 CGD-ASYINT00801-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

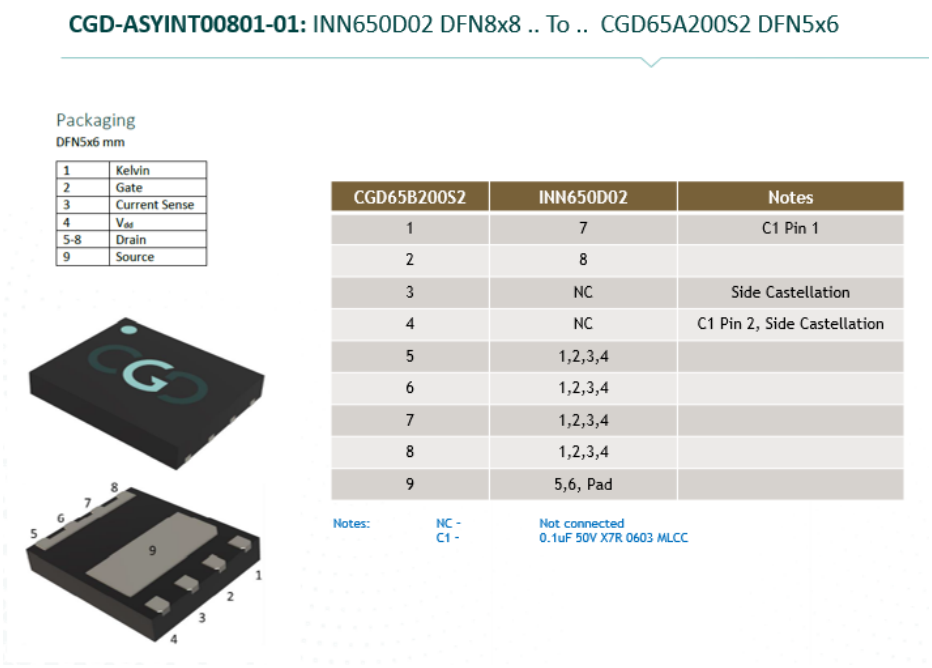


Figure 14 - CGD-ASYINT00801-01 AIB Pin-Definition

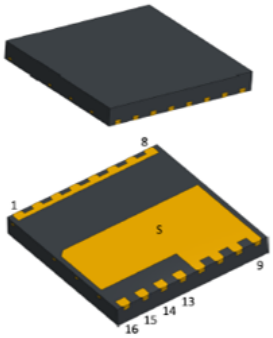
4.9 CGD-ASYINT00901-01 AIB

This AIB does NOT require a separate V_{DD} connection from the customer/recipient PCB.
The AIB/CGD device takes its V_{DD} signal directly from the recipient PCB footprint.

CGD-ASYINT00901-01: NV6125 QFN 6x8 .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{dd}



CGD65A130S2	NV6125	Notes
1	15-23	
2	15-23	
3	15-23	
4	15-23	
5	15-23	
6	15-23	
7	15-23	
8	15-23	
9	2,3,4,5,6, CP	
10	2,3,4,5,6, CP	
11	2,3,4,5,6, CP	
12	2,3,4,5,6, CP	
13	2,3,4,5,6, CP	C1 Pin 1
14	27	
15	NC	Side Castellation
16	28	C1 Pin 2, Side Castellation

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 15 - CGD-ASYINT00901-01 AIB Pin-Definition

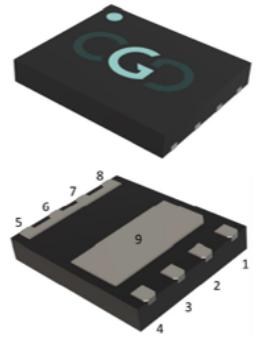
4.10 CGD-ASYINT01001-01 AIB

This AIB does NOT require a separate V_{DD} connection from the customer/recipient PCB.
The AIB/CGD device takes its V_{DD} signal directly from the recipient PCB footprint.

CGD-ASYINT01001-01: NV6125 QFN 6x8 .. To .. CGD65A200S2 DFN5x6

Packaging
DFN5x6 mm

1	Kelvin
2	Gate
3	Current Sense
4	V_{dd}
5-8	Drain
9	Source



CGD65B200S2	NV6125	Notes
1	2,3,4,5,6, CP	C1 Pin 1
2	27	
3	NC	Side Castellation
4	28	C1 Pin 2, Side Castellation
5	15-23	
6	15-23	
7	15-23	
8	15-23	
9	2,3,4,5,6, CP	

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 16 - CGD-ASYINT01001-01 AIB Pin-Definition

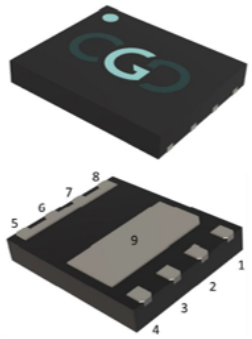
4.11 CGD-ASYINT01101-01 AIB

This AIB requires a separate V_{DD} connection from the customer/recipient PCB to power the CGD device.
Please ensure to connect a safe & secure V_{DD} connection between an appropriate voltage reference node on the customer/recipient PCB design to the appropriate V_{DD} AIB side castellation as shown below.

CGD-ASYINT01101-01: GS-065-011-1-L DFN 5x6 .. To .. CGD65A200S2 DFN5x6

Packaging
DFN5x6 mm

1	Kelvin
2	Gate
3	Current Sense
4	V_{dd}
5-8	Drain
9	Source



CGD65B200S2	GS-065-011-1-L	Notes
1	3	C1 Pin 1
2	4	
3	NC	Side Castellation
4	NC	C1 Pin 2, Side Castellation
5	5	
6	5	
7	5	
8	5	
9	6	

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 17 - CGD-ASYINT01101-01 AIB Pin-Definition

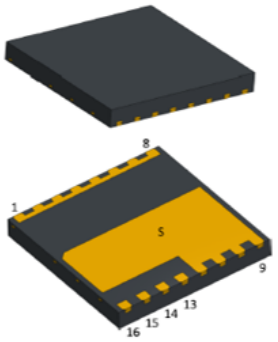
4.12 CGD-ASYINT01201-01 AIB

This AIB does NOT require a separate V_{DD} connection from the customer/recipient PCB.
The AIB/CGD device takes its V_{DD} signal directly from the recipient PCB footprint.

CGD-ASYINT01201-01: NV6128 QFN 6x8 .. To .. CGD65A130S2 DFN8x8

Packaging
DFN8x8 mm

1-8	Drain
9-12	Source
13	Kelvin
14	Gate
15	Current Sense
16	V_{ee}



CGD65A130S2	NV6128	Notes
1	15-23	
2	15-23	
3	15-23	
4	15-23	
5	15-23	
6	15-23	
7	15-23	
8	15-23	
9	2,3,4,5,6, CP	
10	2,3,4,5,6, CP	
11	2,3,4,5,6, CP	
12	2,3,4,5,6, CP	
13	9,29	C1 Pin 1
14	27	
15	NC	Side Castellation
16	28	C1 Pin 2, Side Castellation

Notes: NC - Not connected
C1 - 0.1uF 50V X7R 0603 MLCC

Figure 18 - CGD-ASYINT01201-01 AIB Pin-Definition

Figure List

Appendices

AIB Variants

Table shown correct at document release date although further variants will be added as required.
Please contact CGD for full details.

Recipient Interface			CGD Interface	CGD Ordering Part Number
GaN Systems	GS66508B	GaN_{PX}	DFN 8x8	CGD-ASYINT00101-01
GaN Systems	GS065011-1L	PDFN 8x8	DFN 5x6	CGD-ASYINT01101-01
GaN Systems	GS6530-2L	PDFN 8x8	DFN 8x8	CGD-ASYINT00301-01
Infineon	IPP60R099P7	T0-220	DFN 8x8	CGD-ASYINT00401-01
Infineon	IPP60R099P7	T0-220	DFN 5x6	CGD-ASYINT00501-01
Infineon	IPL60R065P7	ThinPAK 8x8	DFN 8x8	CGD-ASYINT00701-01
Innoscience	INN650D02	PDFN 8x8	DFN 5x6	CGD-ASYINT00801-01
Navitas	NV6115	QFN 5x6	DFN 5x6	CGD-ASYINT00601-01
Navitas	NV6115	QFN 5x6	DFN 8x8	CGD-ASYINT00201-01
Navitas	NV6125	QFN 6x8	DFN 8x8	CGD-ASYINT00901-01
Navitas	NV6125	QFN 6x8	DFN 5x6	CGD-ASYINT01001-01
Navitas	NV6128	QFN 6x8	DFN 8x8	CGD-ASYINT01201-01

Table 2 - All Available Variants of AIB

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