CAMBRIDGE GaN DEVICES

ICeGaN™ – A Novel Technology for Integrated Power GaN

CGD GaN IC Technology

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IN THIS PAPER

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01/03

INTRODUCTION TO GaN POWER DEVICES

COMPARISON OF GaN AND OTHER MATERIALS OF POWER DEVICES

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This white paper describes the features and advantages of ICeGaN™ technology and devices versus alternative solutions in silicon and gallium nitride. The ICeGaN™ devices are the only GaN transistors that feature all the benefits of enhancement discrete GaN High Electron Mobility Transistors (HEMTs), such as ultra-low on-state resistance, zero reverse recovery charges, very low output charges, but have advantageously a high threshold voltage, do not require a negative voltage drive, and can be driven in a similar way to a MOSFET without any additional circuitry and without the need for external clamping circuits. Unlike Cascode devices, ICeGaN™ technology is based on a single GaN die with monolithically integrated sensing and protection functions.

The paper will start by introducing the GaN technology based on the physical properties of the material and making a strong case for its use in power electronics applications. The paper continues with the advantages and peculiarities of the lateral configurations used in HEMTs and gives an overview of the device structures and smart power/Power IC architectures used today. The paper then continues with a compelling case for ICeGaN™, discusses reliability aspects addressed by ICeGaN™ technology, and finishes with the applications of ICeGaN™ in various markets.

GaN INTRODUCTION

Gallium Nitride (GaN) is arguably the most exciting material in the field of power electronics today, enabling the development of high voltage devices with increased power density, reduced on-resistance, and very high frequency response. The wide band gap of the material (Eg = 3.4 eV) results in a high critical electric field (Ec = 3.3 MV/cm), which can lead to designs of devices with shorter drift region, and therefore lower on-state resistance when compared to silicon-based counterparts for the same voltage rating [1].

Table 1 shows the physical properties of different materials vs those of silicon [2]. GaN simultaneously offers higher carrier mobility (for the two-dimensional electron gas – 2DEG), and higher critical electric field than both Silicon and Silicon Carbide (SiC). The availability of relatively inexpensive GaN-on-Si wafers makes GaN a favourite choice among the wide bandgap materials especially in medium-end applications where cost remains a powerful consideration. GaN-

Physical Property	Si	4H-SiC	GaN	SC CVD Diamond	β-Ga_2O_3
Band gap (eV)	1.1	3.2	3.4	5.5	4.9
Relative permittivity	11.9	10	9.5	5.7	10
Breakdown field (MV/cm)	0.3	3	3.3	5	8
Thermal conductivity (W/K/cm)	1.48	3.30	1.30 (GaN substrate) 1.5 (Si substrate) 0.35 (Sapphire) 3.3 (SiC)	24.0	0.13
Mobility ($cm^2/(Vs)$)	1350	700	1200 (bulk) 2000 (2DEG)	3800 for holes 4500 for electrons (intrinsic doping)	200-300
Saturation velocity (10^7cm/s)	1	2	2.5	2	2
Available wafer diameters	8-12″	6″	6-8″ Si		

Table 1 - Material properties of GaN in comparison with Silicon and other wide bandgap materials

on-Si lateral devices are rather suited for relatively lower voltage (40 V to 900 V) and lower power applications (< 10 kW), while SiC vertical devices are best for voltages above 1.2 kV with power levels in excess of 1 kW. GaO and Diamond offer interesting material properties as their bandgaps are wider than those of SiC and GaN, but GaO suffers from poor electron mobility and very low thermal conductivity [3], while Diamond suffers from a lack of effective n-type dopants, fast degradation of mobility at high temperatures, and the lack of shallow dopants (even for p-type) [4]. While GaO and diamond remain an option for the future in specific applications, it is expected that GaN and SiC would make a strong market penetration in the next 10 years.

"Gallium Nitride (GaN) is arguably the most exciting material in the field of power electronics today"

FLORIN UDREA

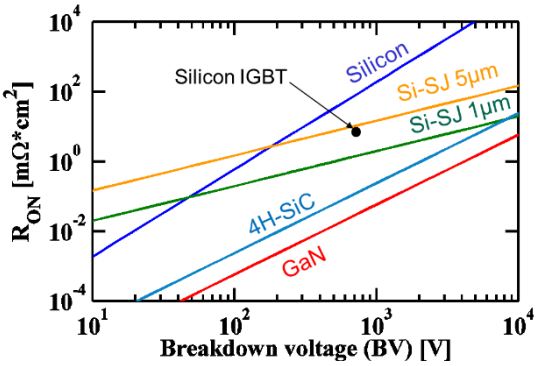

Figure 1 - Specific Ron vs breakdown voltage limits for different materials and technologies.

Both Baliga FOM (Figure of Merit) and Johnson FOM for GaN and SiC, shown in Table 2, are orders of magnitude higher than those of Silicon making a strong case for the use of these materials in power semiconductor devices in order to improve the efficiency of power systems and/or reduce their form factor by operating at higher frequencies. Recently the FOMs for different materials have been adjusted to take into account 2D and 3D superjunction design and the parasitic JFET effect within the superjunction pillars [5], [6]. This led to a slightly different dependence of the specific on-state resistance, Ron with the critical electric field, Ec (Ron ~ $1/Ec^{2.5}$ rather than $1/Ec^3$).

A graph displaying the on-state resistance, Ron, vs breakdown limits is a powerful and well-established way to assess different technologies and materials (Figure 1). These limits are closely related to the static figures of merit. The original limit of Silicon is based on a one-dimensional Power MOSFET design, and no longer represents an "ideal" case as this has been invalidated by the theory of super-junction [6]. The original limits for wide bandgap materials are shown in Figure 1. The superjunction Silicon limits for a 5 and 1 micron cell pitch are also plotted, showing the ability of silicon to out-perform its one-dimensional limit. However, one can note that even when pushing the super-junction concept to the limits (with very aggressive narrow pillars), there is still enough ground to justify the development of wide bandgap materials such as SiC and GaN. Besides this, both SiC and GaN can further improve their corresponding limits by

Figure of merit (FOM)	Si	4H-SiC	GaN HEMT	SC CVD Diamond	β-Ga_2O_3
Baliga's FOM	1	134	537	141635	3571
Johnson's FOM	1	20	27.5	74	27

Table 2 - Figures of merit (FOM) for GaN and other wide bandgap materials relative to Silicon

employing various forms of superjunction [6]. The graph in Figure 1 also shows that GaN offers a better static trade-off than its SiC rival. Nevertheless, for a more detailed picture, one should consider other factors such as maturity of technology (in favour of SiC), thermal conductivity (in favour of SiC), channel resistance (in favour of GaN), and wafer size and CMOS infrastructure (in favour of GaN for lateral devices).

LATERAL VERSUS VERTICAL CONFIGURATION

The use of an AlGaN/GaN heterostructure in lateral GaN devices allows the formation of a two-dimensional electron gas (2DEG) at the hetero-interface, where carriers can reach very high mobility (μ = 2000 $cm^2/(Vs)$) values [1]. This is because the 2DEG acts as a quantum layer where electrons can move fast without scattering from neighbouring ion impurities. Transistors in this technology are named High Electron Mobility Transistors (HEMT). In addition, the piezo-polarization charge present at the AlGaN/GaN heterostructure results in a high electron density in the 2DEG layer (e.g. $1x10^{13}$ cm^{-2}) [7]. These properties allow the development of transistors with unique and very competitive performance.

The lateral configuration has also some attractive features compared to the vertical configuration. It allows:

- monolithic integration of sensing, protection and drive circuits with relatively simple isolation and efficient shielding between different components
- easy access to all terminals (including the high voltage terminal)
- integration of half bridge devices and multiple power devices operating on a common substrate
- the connection of the substrate to the ground and its physical contact to a heat sink
- simple hybrid integration with silicon devices via surface wire bonding
- simpler and cheaper packaging
- devices to be self-terminated (i.e. do not require an additional termination region to shape the electric field at the edge of the device as in the case of vertical structures)

The vertical configuration remains however a preferred option for higher power levels. At higher power levels (>1.2 kV and above 10 kW), the competition from SiC should not be underestimated. GaN indeed can offer some advantages in terms of its high critical electric field and higher channel mobility, but SiC presents a native gate oxide and its dopants are shallow (in the bandgap) and very well controlled. A good review of vertical GaN technologies and prospects can be found in [8].

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GaN DEVICES AND LEVELS OF INTEGRATION

FROM DISCRETE DEVICES TO GaN POWER IC

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Now and over the next decade, lateral GaN devices will exist in different voltage ratings from 40 V to 900 V. In particular the classes of 30-40 V, 100 V, 200 V, 600-700 V, and 900 V are very popular.

There are several types of HEMT-based discrete power devices and power integrated circuits in the market (or close to entering the market) today. Examples of devices and technologies from a number of companies are given below.

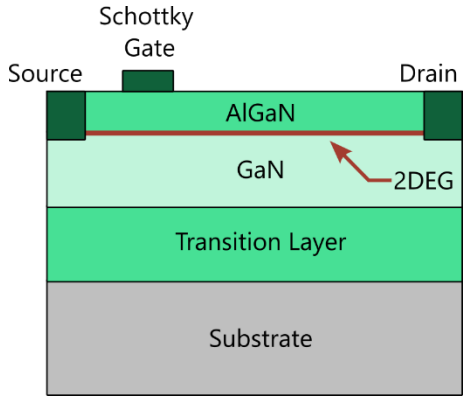
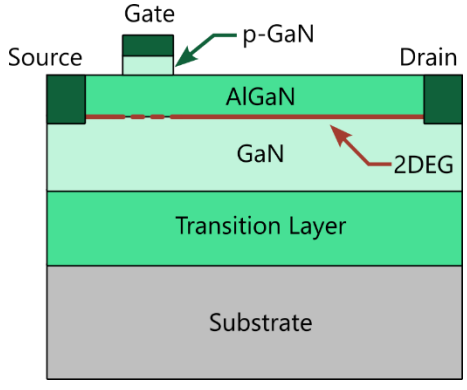
Discrete or Discrete-like devices

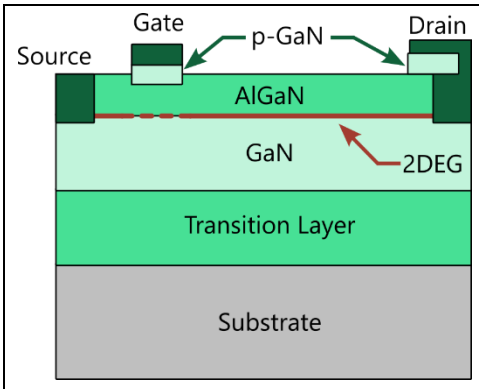
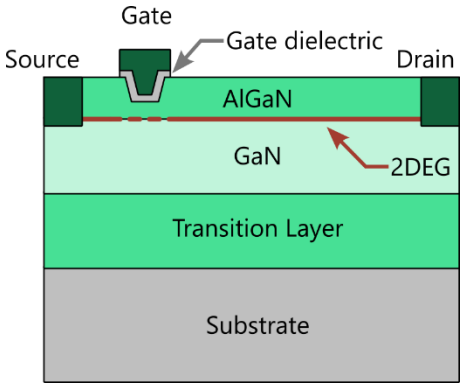
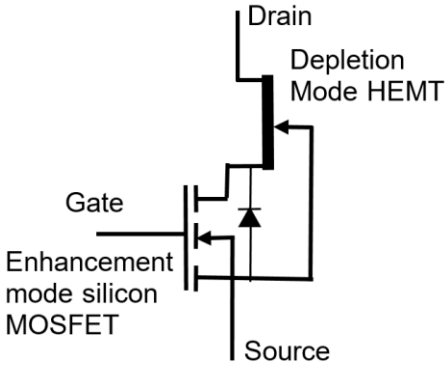
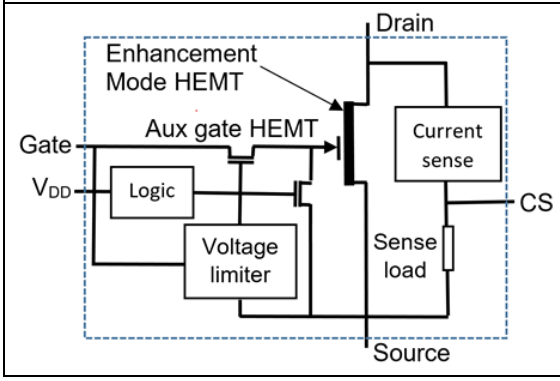
- Cascode technology based on a high voltage depletion HEMT on GaN-on-Si and an enhancement low-voltage MOSFET
- Series connection of Si MOSFET with high voltage depletion HEMT with direct access to the HEMT gate and additional Si circuitry
- Enhancement mode p-GaN HEMT on Si substrates

Power IC and System on Chip devices

- Hybrid integration of Silicon drives/controller and enhancement HEMTs on GaN on Si
- Hybrid integration of Si drives and controllers with GaN on Si or on Sapphire
- Monolithic integration of smart interfaces for sensing/protection, ease of use and enhanced gate reliability
- Monolithic integration of gate drive and sensing circuits

Table 3 shows some of these solutions with features and challenges. The first 4 rows present the schematic cross-sections of different GaN HEMTs used today. The final 4 rows present configurations where such devices are used to enhance their performance, safe operating area and ease of use. What transpires is the diversity that GaN offers today to provide tailored solutions for different applications in power electronics. From the simplicity of enhancement GaN discrete transistors to the complex half-bridge monolithic integration with logic and drive circuits, GaN offers several layers of complexity to maximise its benefits against Silicon solutions.

	**DEPLETION MODE HEMT** Features: (i) Vth negative, normally-on operation, (ii) low Ron. Challenges: (i) limited use as a stand-alone device; used mainly in a Cascode configuration, (ii) Schottky gate voltage cannot go beyond +0.8 V, (iii) requires negative gate voltages for the turn-off.
	**ENHANCEMENT MODE P-GaN GATE HEMT** Features: (i) normally-off operation, (ii) p-GaN gate using Mg doping, (iii) choice of gate Ohmic contact on the p-GaN (for enhanced gate reliability) or Schottky contact (for reduced leakage current). Challenges: (i) low threshold voltage Vth ~ 1.5 V, (ii) fragility of the gate with max voltage ~7 V, (iii) requires negative voltages for a safe and reliable turn-off.

	**GATE INJECTION HEMT WITH ADDITIONAL P-GaN HOLE INJECTOR CONNECTED TO DRAIN** Features: (i) similar to the p-GaN HEMT based on Ohmic gate contact, (ii) enhanced reliability provided by the p-GaN hole injector connected to the drain, (iii) thicker AlGaN under the hole injector compared to that under the gate, to avoid depletion of the 2DEG. Challenges: same as p-GaN HEMT
	**ENHANCEMENT MODE MIS HEMT** Features: (i) recessed insulated (MIS) gate for positive Vth, (ii) low gate leakage, (iii) extended gate voltage range. Challenges: (i) reliability of the gate given traps and interface states, (ii) reproducibility and stability of the threshold voltage, (iii) hot carrier injection from AlGaN into the gate dielectric, (iv) high electric fields at the corner of the trench gate dielectric.
	**CASCODE DEVICE** Features: (i) depletion mode HEMT in series with a low-voltage enhancement-mode Silicon MOSFET, (ii) stable, reliable and easy to use drive provided by the silicon MOS gate, (iii) good reliability, (iv) low on-state forward drop in the reverse conduction (diode) mode (3rd quadrant) Challenges: (i) co-packaging of two or multiple components, (ii) voltage sharing, (iii) reverse recovery losses due to the anti-parallel bipolar diode, (iv) no possibility of adjustment of slew rate on the HEMT gate, (v) relatively high output charge
	**SMART HEMT (ICeGaN™ HEMT)** Features: (i) monolithically integrated smart sensing and protection circuits, (ii) stable, reliable and easy to use drive provided through a GaN interface attached to the gate, (iii) high Vth ~ 3 V, (iv) extended voltage range up to 20 V, (v) no negative voltage requirement

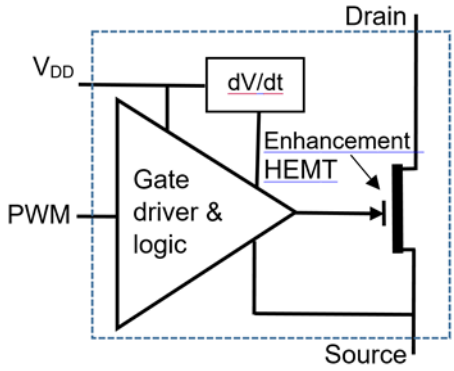
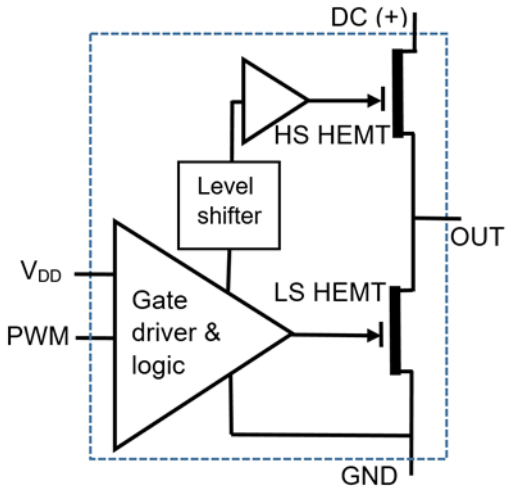
	(vi) current sensing, (vii) Miller clamp for safe turn-off and gate protection, (viii) integrated ESD. Challenges: (i) extra GaN area for the smart interface.
	**POWER IC WITH HEMT AND INTEGRATED DRIVE** Features: (i) monolithically integrated drive & logic circuits with slew rate control, (ii) stable & reliable operation, (iii) compact solution. Challenges: (i) extra GaN area for the drive circuit, (ii) thermal consideration, as the drive & logic circuits can get hot during HEMT operation, (iii) limited performance of the drive and logic circuits - availability of only n-channel low-voltage GaN transistors (no p-channel devices).
	**POWER IC WITH HALF-BRIDGE INTEGRATION** Features: (i) Low-side HEMT integrated with high-side HEMT in half-bridge, (ii) driver, logic and level shifter circuits monolithically integrated, (iii) compact solution and low parasitics. Challenges: (i) extra GaN area for the circuits, (ii) thermal consideration, as the drive and logic circuit can get hot during operation of the half-bridge, (iii) limited performance of the drive and logic circuits - availability of only n-channel low-voltage GaN transistors (no p-channel), (iv) interference between LS and HS HEMTs.

Table 3 - GaN Power Devices and Architectures

03/03

ICeGaN™ TECHNOLOGY

FUNCTIONALITY, RELIABILITY AND IMPLEMENTATION OF CGD'S GaN IC

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The technology's name ICeGaN™ stands for "Integrated Circuit Enhancement GaN". It is a platform based on an enhancement GaN HEMT that is aimed at running cooler than other "cool(MOS)" solutions, due to its ultra-low specific on-state resistance and very low capacitances.

ICeGaN™ TECHNOLOGY IN A NUTSHELL

ICeGaN™ can be driven in a similar manner to a silicon MOSFET and unlike all other enhancement GaN solutions, it is compatible with any silicon-based driver. Its zero reverse recovery losses and very low output charges make it an ideal choice for high frequency, high-efficiency applications.
Presently there are two approaches in the market (i) discrete p-GaN approach and (ii) monolithic approach where the gate driver is fully integrated. Both these solutions have their own shortcomings. The low threshold voltage (~1.2 V for Ohmic p-GaN gate solutions and 1.7 V for Schottky p-GaN gate devices) specific to p-GaN enhancement mode devices [9] requires negative drive voltages to limit false turn-off events of the HEMT during high dV/dt transients [10]. The full driver integration, on the other hand, while providing reduced parasitics, takes away the flexibility of using low-cost, high-performance silicon-based drivers, or gate drivers integrated with powerful controllers. Additionally, due to on-chip thermal coupling, the gate driver can suffer from extra losses due to the self-heating of the power device. Scaling up a fully integrated solution to higher power levels is also questionable.

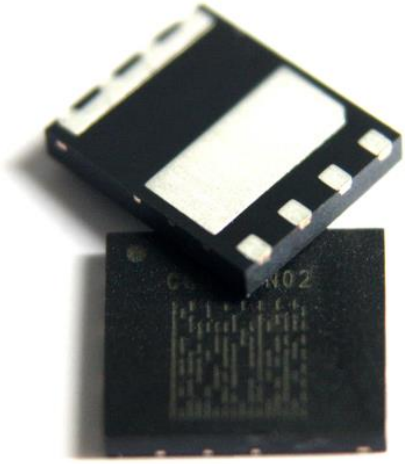

Figure 3 – ICeGaN™ Device packaged in a 5x6 mm DFN package. Larger Devices are packaged in an 8x8 mm DFN.

In contrast, the ICeGaN™ devices have a higher threshold voltage, Vth ≈ 3 V in order to suppress dV/dt related spurious turn-on events and as a result, allow safer operation. Moreover, the ICeGaN™ devices can be driven with gate voltages of up to 20V (well in excess of the standard 7V for p-GaN HEMTs [11]) without any compromise in the device transconductance or dynamic performance.
Figure 3 shows a photograph of the ICeGaN™ packages. An example of an ICeGaN™ chip is shown in Figure 4. A block description of an ICeGaN™

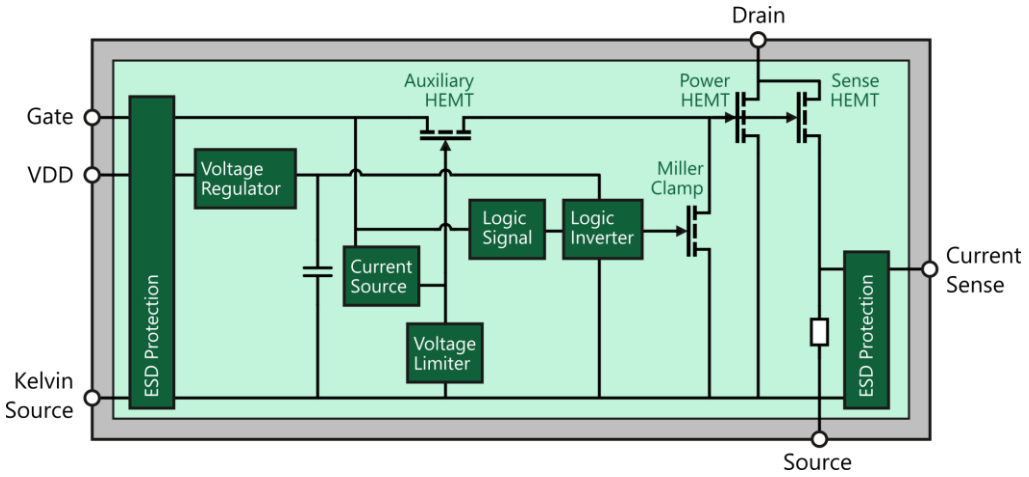

Figure 2 - ICeGaN™ monolithically integrated circuit which comprises a smart gate interface and a current sensing function using a sense HEMT.

device which includes the main HEMT, the sense HEMT, the sensing load and a circuit diagram of the ICeGaN™ smart interface is shown in Figure 2.

Figure 4 – ICeGaN™ Power HEMT featuring a smart interface and a tapered design of the source/drain metallisation for optimum current distribution.

ICeGaN™ KEY FEATURES

i) HIGHER THRESHOLD VOLTAGE AND HIGHER VOLTAGE RANGE

One of the key advantages of the Cascode solutions is the high threshold voltage (2.3 - 3.5 V) and the high voltage range (0-20 V) offered by the silicon MOSFET (connected in series with the depletion HEMT). However, this involves a multi-component package and therefore additional cost. Moreover, the Cascode combination has a higher output charge than a single die enhancement HEMT. Furthermore, the Cascode cannot claim zero reverse recovery losses, one of the key advantages of lateral GaN HEMTs over silicon superjunctions.

In contrast, ICeGaN™ devices have advantageously high threshold voltage (3.0 V) – see Figure 5 – high voltage range (0-20 V) (specific to Cascode) but also zero reverse recovery losses and very low output charge (specific to enhancement GaN HEMTs).

ii) MILLER CLAMP

One of the important features of ICeGaN™ devices is the monolithically integrated Miller Clamp. The clamp has a dual purpose (i) to keep the device safely in the off-state even during fast switching events or external transients, and (ii) to provide a fast turn-off of the main HEMT when the clamp is on.

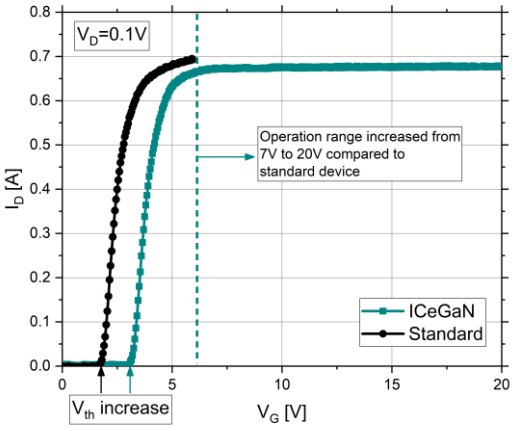

Figure 5 - Transfer characteristic of a standard p-GaN HEMT vs an ICeGaN™ device which shows an increased Vth and a wider gate window of operation.

iii) CURRENT SENSING

In many power electronics circuits, the current through the switching transistor needs to be measured continuously to provide the required input for the control chip. With conventional Silicon MOSFETs and GaN transistors, this is done by adding a sense-resistor in series with the transistor, as shown in Figure 6. The current through this resistor causes a voltage drop of typically up to 1 V; this voltage signal is used for the control circuit.

ICeGaN™ devices have a monolithically integrated current sense function on the chip which eliminates the need for this series resistor (see Figure 9).

This solves all three major disadvantages of the conventional arrangement. In conventional solutions, the whole current to be sensed is flowing through the additional resistor. This is lossy and reduces system efficiency. CGD's solution reduces these losses to a fraction, as shown in Figure 10.

The source of the CGD transistor is on the electrical ground potential of the converter, as opposed to the current sense potential. This solves the second problem of conventional current sensing, the additional electrical noise and coupling generated by the voltage difference between the source of the transistor and ground. Since electromagnetic compatibility is a very important parameter of a power system which is difficult to improve, this

provides a key advantage on the system level and reduces the design-in time for ICeGaN™ devices.

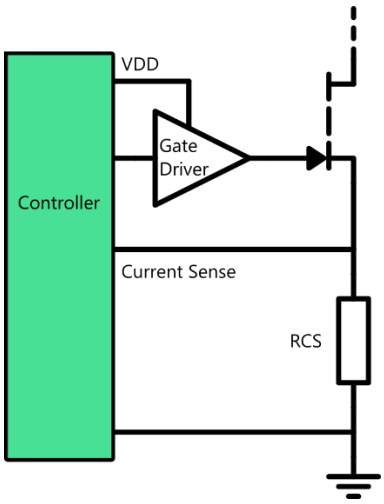

Figure 6 - Conventional current sensing arrangement. The transistor current is flowing through RCS and the resulting voltage drop is the current sense input of the controller.

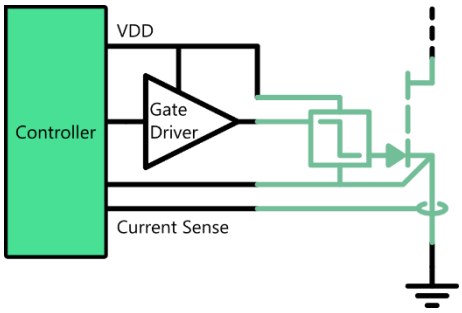

Figure 9 - CGD's integrated current sensing function, where the current sense signal is generated on the GaN IC.

The third issue solved by the current sensing in ICeGaN™ devices concerns the heat extraction. As mentioned, in ICeGaN™ devices, the source of the main HEMT has the same electrical potential as the ground. This means that the ICeGaN™ devices are directly thermally connected to the ground plane. The ground plane of the system is the largest copper on the system PCB, therefore ideally suited to extract and spread the heat from the device. This is shown in Figure 7 and Figure 8.

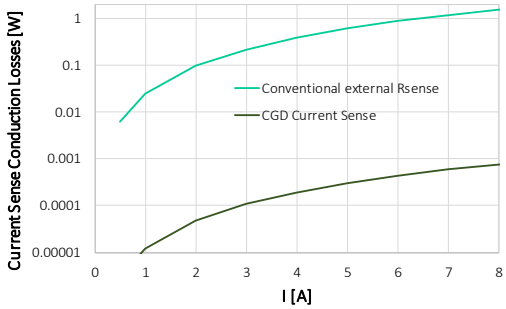

Figure 10 - Comparison of the typical losses caused by current sensing in a conventional circuit and when using the CGD solution. The CGD solution virtually eliminates the losses.

iv) ESD PROTECTION

An ESD protection circuit is monolithically integrated within the ICeGaN™ smart interface. This is based on a charge sensitive HEMT which absorbs any excessive energy when any external pin of the ICeGaN™ is subjected to an ESD event.

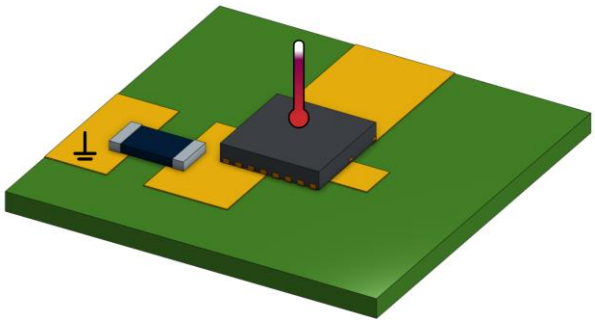

Figure 7 - Conventional current sensing arrangement with a shunt resistor between ground and the transistor. Thermal resistance from junction to ground plane increases affecting heat dissipation.

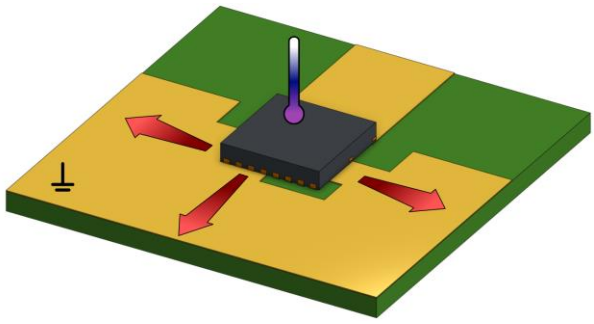

Figure 8 - In ICeGaN™ devices, the integrated current sensing through a sense HEMT allows the main HEMT to be thermally connected to the large ground plane, ideally suited to spread and extract the heat.

v) ICeGaN™ DRIVE

Unlike conventional enhancement GaN HEMT devices which use either Schottky or Ohmic p-GaN gates, ICeGaN™ does not require extra Zener diodes to clamp the gate drive voltage and does not require negative gate voltages to switch the device off. Magnetic beads are also not necessary, thus cutting the cost of the system solution. ICeGaN™ can be simply driven as shown in Figure 11 for a single low-side device and Figure 12 for a half-bridge.

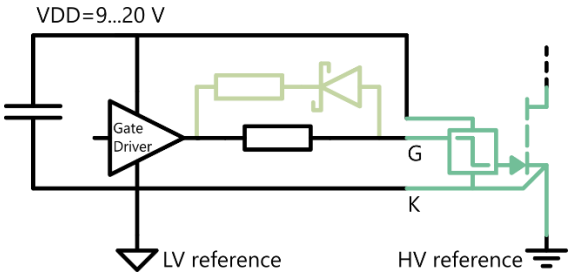

Figure 11 - Low-side transistor drive of an ICeGaN™ device. The turn-off path with a Schottky diode and a resistor is optional and allows a faster slew rate for turn-off compared to turn-on.

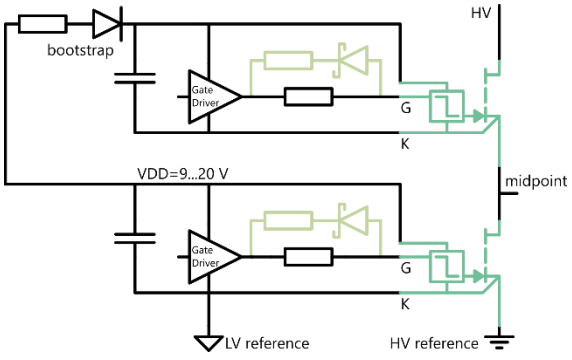

Figure 12 - Half-bridge drive of ICeGaN™ devices featuring a bootstrap circuit for high-side supply of the gate drive voltage.

An example of Bill of Material (BOM) of external components involved in driving ICeGaN™ vs a conventional/competitor solution is captured in Table 4. ICeGaN™ results in a simpler and more economical solution.

Function	Competitor		CGD
Control turn-on speed	2 x resistors	5-10 Ω / 1% 200 mW	Same
Keep the driving voltage	2 x resistors	10 kΩ / 5%	Not needed
Hold negative voltage for turn-off	2 x capacitors	47 nF / 30 V	Not needed
Zener diode to clamp positive V_G	2 x Zener diodes	5V6 200 mW	Not needed
Zener diode to clamp negative V_G	2 x Zener diodes	5V6 200 mW	Not needed
VDD voltage supply	Not needed		2 x capa-citors

Table 4 - Typical BOM comparison of a system featuring CGD ICeGaN™ with conventional GaN devices

ICeGaN™ VERSUS SILICON SUPERJUNCTION AND OTHER GaN SOLUTIONS

The key combined static and dynamic FOMs and key features of ICeGaN™ compared to Silicon Superjunction and other types of state-of-the-art GaN devices are shown in Table 5. ICeGaN™ offers a set of very compelling performance advantages against the best of silicon (Superjunction devices) and other GaN competing devices. The high threshold voltage of ICeGaN™ and the possibility of operating at high gate voltages are unique among the single-die GaN technology, providing an enhanced safe operating regime. The combination of very low specific on-state resistance with low output charge and zero recovery losses makes it a very attractive proposition in the market.

RELIABILITY OF GaN DEVICES IN GENERAL AND ICeGaN™ IN PARTICULAR

The field of power electronics is experiencing a major and exciting change with the adoption of wide bandgap semiconductors. GaN is currently seeing an exponential increase in demand. Its attractiveness in the market comes from the excellent performance benefits as a result of its enhanced physical properties compared to those of Silicon. For system designers, GaN devices have the ability to operate at higher frequencies, which can cut the size, volume, and ultimately the cost of passives (transformers, inductors and capacitors), while still benefiting from higher system efficiency, thus reducing the cost of the heat sink, or, in some specific cases, eliminating the need for thermally enhanced PCBs. However, one area where Silicon still has the edge is reliability.

There were several potential concerns for the reliability of GaN, most of which have now been largely addressed while others are in the process of being overcome.

i) VERTICAL LEAKAGE

The vertical leakage current from the drain of a lateral GaN HEMT to the semiconductor substrate used to be a major concern in the past. The quality of the epi layers (nucleation layer, the transition layer and the buffer) has been tremendously improved, and the vertical leakage (though still dominant at very high blocking voltages) has been reduced by orders of magnitude and is no longer a major problem.

ii) DYNAMIC RON

The 2DEG which inherently exists at the AlGaN/GaN hetero-interface has been found to be unstable and lose electron charge when a prior high voltage stress was applied. This phenomenon is known as dynamic Ron or current collapse. When the device is under high voltage stress in the off-state, a fraction of the electrons in the 2DEG is lost by trapping mechanisms in either traps in the bulk of the GaN, the transition layer (i.e. the layer placed between the substrate and the GaN buffer) or at the surface of the device. Hot carrier injection in the passivation layer, next to the gate (the control terminal) also may play a role, though this is not believed to be the major contribution to the dynamic Ron phenomenon. This loss of charge from the 2DEG layer to the surrounding traps leads to a subsequent decrease in the conductivity during on-state, and thus an increase in the on-state

	Silicon Super-junction	GaN Cascode	p-GaN gate Ohmic HEMT	p-GaN gate Schottky HEMT	ICeGaN™
Specific on-resistance Ron.Area [mΩ.cm^2]	8	2.8*	3.2	3.2	3.2
Threshold voltage [V]	3.5	4.0	1.2	1.7	3.0
Maximum gate voltage [V]	20	20	6	7	20
Ron.Qg [mΩ.µC]	3.5	0.8	0.32	0.3	0.33
Ron.Qoss [mΩ.µC]	21	6	2.3	3.3	3.6
Ron.Qrr [mΩ.µC]	312	6	0	0	0
Negative voltage drive requirement	No	No	Desirable	Desirable	No
Current sensing	No	No	No	No	Yes
Typical packaging	TO-247	TO-247	DFN	DFN	DFN

*) Includes only the Depletion GaN HEMT (excludes the Silicon FET in series)

Table 5 - Features of Silicon super junction MOSFETs and various gate drive implementations of GaN devices, including ICeGaN™

resistance. The effect could be seen also during the switching or when the device is in operation in a real system.

The hot carrier injection and the trapping effect of the electrons in the bulk of the GaN or at the surface of the device, in the vicinity of the gate, leads not only to a loss in the 2DEG layer conductivity, but is also associated with a shift in the threshold voltage. The trapping and the hot carrier injection are significantly more prominent at higher electric fields. One of the peaks of the electric field occurs at the drain side of the edge of the gate structure.

There are two possible ways to minimise the effect of the dynamic increase in the on-state resistance: (i) use of field plates in order to reduce the field peaks in the structure, in particular around the gate structure, to minimise the effect of electron trapping from the 2DEG and/or hot carrier injection [12]. Another approach is (ii) the use of a hole injector layer to inject holes into the bulk and actively passivate the bulk traps [13]. There are several theories describing the effect of the injected holes. One possible mechanism is that the injected holes change the electric field distribution from the 2DEG to the substrate, by moving the high fields away from the 2DEG vicinity, towards the substrate. As a result, the 2DEG is exposed to lower electric fields which slows down the mechanism of electron trapping in the vicinity of the 2DEG [14].

The Dynamic Ron has been greatly reduced today with most GaN chip manufacturers guaranteeing a maximum of 20-30% increase in Ron while others claiming a negligible increase (below 10%). In the next five years, it is entirely possible that this problem would be solved completely.

The dynamic Ron performance of ICeGaN™ is similar to that of state-of-the-art enhancement-mode GaN devices using a p-GaN Schottky gate.

iii) FRAGILITY OF THE GATE

The p-GaN gate, using Magnesium doping is considered today the most promising solution for an enhancement HEMT. It delivers a normally-off operation with a relatively low positive threshold voltage of 1.3 V to 1.6 V. The gate cannot be biased above 7 V with respect to the source as the gate current increases exponentially.

The Cascode and the ICeGaN™ devices have been introduced to address exactly these problems, achieving a higher threshold voltage and a gate range similar to those offered by Silicon devices (e.g. 3 V and up to 20 V respectively).

The threshold stability has also been found to be affected by traps in the p-GaN, AlGaN and at the interface between the two. In general, an Ohmic gate placed on the p-GaN offers a more robust solution, but a Schottky contact has the benefit of a lower gate leakage current. The latter is particularly important at high temperatures.

The fragility of the gate can also be addressed by integrating the driver or adding protection (clamping) circuits.

The ICeGaN™ features an auxiliary gate low-voltage transistor (Figure 2) that absorbs a certain amount of the external gate voltage during the turn-on and on-state operation, thus protecting the device against extreme gate voltages. The amount absorbed is also temperature dependent, to further improve the reliability of the p-GaN gate. It is known that the gate is more fragile at very low temperatures (e.g. -40°C) and the maximum voltage applied to a gate of the HEMT should be lowered at lower temperatures [15] [11]. In conventional solutions this cannot be done as the voltage applied to the gate of the HEMT is not controlled with respect to the operating temperature. In contrast, in ICeGaN™ devices, the auxiliary gate transistor is configured to absorb a higher voltage drop at lower temperatures thus clamping the maximum voltage on the internal gate to a lower potential (below 5.5 V) hence improving very substantially the reliability of the device.

ICeGaN™ MARKET

ICeGaN™ is a highly scalable technology. Its potential voltage range is from 100 V to 900 V and power levels from 40 W to 10 kW. Currently, Cambridge GaN Devices focuses on 650 V devices with specific Ron levels of 200 mΩ, 130 mΩ, and

55 mΩ, corresponding to power levels of 60 W to 4 kW, depending also on the package choice.

There are a number of applications that would benefit from the fast frequency and low on-state losses of ICeGaN™, such as AC to DC chargers, power supplies (e.g. for smartphones, laptops, gaming consoles or PCs), lighting (e.g. LED drivers), UPS, wireless power, on board chargers and HV DC to DC converters for electric vehicles, and datacentres. New applications in telecom systems, AI (artificial intelligence systems) and cryptocurrency mining are also emerging.

Motor control applications currently use conventional silicon devices. In particular, the Insulated Gate Bipolar Transistors (IGBTs) have been very successful in this field. Nevertheless, IGBTs do not naturally have reverse conduction, and they tend to struggle as the operating frequency is increased (above 20 kHz). Other GaN solutions based on a Cascode solution have the disadvantage of relatively high reverse recovery losses. Enhancement GaN HEMTs need extra external circuits for clamping and negative voltages for switching off. Here ICeGaN™ can make a strong impact due to its ease of drive, using any silicon-based half-bridge driver and its zero reverse recovery losses.

The key combined static and dynamic figures of merit (FOM) and features of ICeGaN™ result in compelling system performance advantages against those using the best of silicon (Superjunction devices) or other GaN solutions. It is also interesting to note that GaN is evolving significantly faster than Silicon. Silicon is already a very mature technology and its performance is at best incrementally enhanced from year to year. GaN, on the other hand, is in a phase where its key performances are enhanced dramatically. This trend is set to continue for the next decade widening the performance gap between GaN and Silicon.

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