350 W TOTEM-POLE PFC EVALUATION BOARD

with CGD65A055SH2

USER GUIDE

CGD – UG2402

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CGD™
CAMBRIDGE GaN DEVICES

Safety Warning

The CGD totem-pole power factor correction (TPPFC) evaluation board (EVB) is for evaluation purposes only. It is not intended to be a finished product and does not include all protection features found in a commercial power supply.

DANGER: Do not touch the board when high voltages are applied. There are exposed locations of high voltage on the board when connected to a power source. Brief contact may result in serious injury or death. Allow all components to fully discharge before handling the board. This evaluation kit is designed for use by qualified, experienced engineers only. Appropriate safety measures must be put in place before use and the board should never be left unattended.

WARNING: Some components may become hot during operation and remain so afterwards. Operating voltages, currents and temperatures should be monitored closely throughout operation to prevent damage to the board.

CAUTION: This product contains parts susceptible to ESD (electrostatic discharge). ESD prevention procedures must be used while handling the board.

Operating Limits and Recommendations

Voltage, current and power limits

CGD has tested the board within the following ranges: input voltage range of 90–265 V_{AC} 47–63 Hz, output voltage 395 V, rms output current 0 – 0.89 A. This evaluation board is for demonstration purposes only and should not be used to power any loads other than an electronic load. Only trained professional using high voltage equipment should operate the board and appropriate safety precautions should be followed.

Heat dissipation

This is an open frame design. CGD makes no guarantee of the thermal performance.

Do not touch the circuit components until the components cool down after turning off. In full-load conditions, temperatures of certain circuit components like totem-pole PFC ICeGaN™ devices, magnetics and MOSFETS could rise up beyond of 80 °C after 20 minutes of operation, with ambient temperature 25 °C. Therefore, it is recommended to use a thermal camera to monitor the circuit temperature during circuit operation and turn off the circuit if the temperatures rise above nominal operating temperatures.

Target Audience

This user guide, along with the evaluation board, is intended to be used only by experienced engineers and assumes a knowledge of necessary equipment to analyse the performance of the circuit board. It is designed to enable SMPS engineers, design engineers and technicians involved in the development of a power electronics system to assess the performance of CGD ICeGaN devices.

Technical Support

For support, please contact CGD at techsupport@camgandevices.com.

Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Issue	CT	19/02/2024

Contents

1 Introduction

This user guide provides basic information about the 350 W TPPFC evaluation board designed by CGD, a 350 W (396 V at 0.89 A) universal input offline power converter (90 V_{AC}-265 V_{AC}), and serves as a manual to understand and operate the board.

The evaluation board allows users to evaluate the ICeGaN device CGD65A055SH2. This device is a CGD's H2 series device. It is a 650-V 55-mΩ enhancement-mode GaN (e-GaN) device with proprietary ICeGaN technology. ICeGaN is CGD's gate technology for high gate threshold and broad gate voltage window compatible with gate-driver ICs designed for Si MOSFETs.

The EVB's topology is a critical conduction mode (CrCM) bridgeless totem-pole PFC. The evaluation board consists of two PCBs: a motherboard and daughterboard. The motherboard includes all the components except the TPPFC fast leg, which is implemented in the daughterboard, to facilitate testing of the ICeGaN devices.

The CrCM TPPFC controller used in this evaluation board is the NC1680. This controller is well supported with technical documentation and design tools. The design equations for the TPPFC are well known and out of the scope of this user guide.

The contents of this user guide include key specifications, EVB description, test set up, test results, key waveforms, circuit schematics, PCB layout, magnetics datasheets, and bill of materials (BOM) of the CGD 350 W TPPFC evaluation board.

Table 1 – Key specifications

Description	Value	Unit
Input ac line voltage range	90 - 265	V
Input ac line frequency range	47 - 63	Hz
Output voltage	395	V
Output current	0.89	A
Maximum output continuous power	350	W
Maximum peak-to-peak output ripple	< 5	%
Power Factor (PF) at maximum load over the input voltage	> 0.95	
Total Harmonic Distortion (THD) at maximum load over the input voltage	< 10	%
Peak efficiency	> 98	%
Efficiency at 90 V_{AC} / Full load	> 92	%
Average four-point efficiency at 115 V_{AC}	> 97.5	%
Average four-point efficiency at 230 V_{AC}	> 98.5	%
Board dimensions (with daughterboard inserted)	206 x 114 x 75	mm

2 Board Description

The CGD 350 W TPPFC evaluation board is designed to easily check various signals, learn more about how the TPPFC works, and see first-hand the advantages of using ICeGaN in such a topology.

The slow leg employs N-Channel 67 mΩ 650 V MOSFETs (TO-220) to minimize the conduction losses. The UCC27712, a standard MOSFET 650V half bridge gate-driver IC has been selected to drive these MOSFETS.

The fast-leg half bridge is implemented on a daughterboard and uses two CGD65A055SH2 ICeGaN devices driven by the same gate-driver IC used for the slow leg MOSFETs. ICeGaN has an internal Miller Clamp for turn off, thus only an external gate resistor is necessary for each ICeGaN. Nevertheless, the evaluation board provides placeholders for additional turn off components (resistor and diode) in parallel with the gate resistor. CGD's ICeGaN simplifies the driving of the GaN HEMTs; there is no need of a negative gate drive or specific GaN driver which reduces complexity and part count.

The CrCM PFC topology operates with fixed on-time and variable switching frequency that depends on the input voltage and output load. The PFC inductor selected is a 130 µH inductor which sets a minimum switching frequency of approximate 50 kHz at low line and full load conditions. This inductor has an auxiliary winding which gives information about the voltage across the inductor to the NCP1680 controller.

The bulk capacitor consists of two parallel 120 µF / 450 V electrolytic capacitors in parallel. With such value the low frequency output voltage ripple (100 Hz /120 Hz) is less than 5% peak-to-peak.

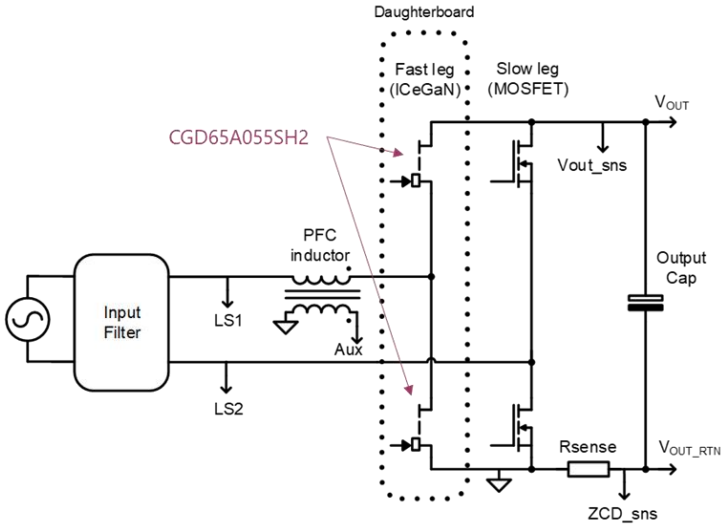


Figure 1 – CGD 350 W TPPFC EVB functional schematic

The NCP1680 controller requires a current sense resistor placed between the negative terminal of the electrolytic bulk capacitor and the source of the low-side MOSFET and ICeGaN device, see Figure 1. This resistor is called R_{ZCD} and it is formed by the parallel combination of R42, R44 resistor. It is used for zero current detection and overload detection. For more details check the NCP1680 datasheet.

3 TEST SET UP

The motherboard and daughterboard are shown below in Figure 3 and Figure 4 respectively. To help operate the board, and make testing easier, the motherboard includes multiple I/O connectors which are described in Table 2 as well as test points listed in Table 3. In the same fashion, the daughterboard includes multiple test points and MMCX connectors listed in Table 4.

Below, some important points are highlighted to run the evaluation board correctly and safely:

1. J7 - The daughterboard must be inserted in J7 in the correct position shown in Figure 2.

2. J1 - The evaluation board requires an external low voltage rail (12–15 V), provided on J1 (see all the I/O connectors in Table 2), to power the control circuitry. The evaluation board includes the option to generate the low voltage rail through a diode that rectifies the PFC inductor's auxiliary winding voltage. However, this functionality has not been tested and all the testing performed by CGD has been carried out providing 12 V externally through the connector J1.

3. J6 - The pin 2 of the input connector J6 is mains earth and it is marked in the PCB as CHGND. This connection is not required and can be left open. The user should determine the appropriate input connection based on their application requirements.

4. J3 – Only used for no-load power testing. The controller's *Skip* mode, described below, can be activated manually by shorting J3. On the other hand, J3 must be always open to allow normal operation. In a typical application this control signal would be provided by a downstream dc−dc converter. CGD's no-load results shown in section 4.2 No load power were recorded with J3 shorted.

   Important: *Skip* mode must never be activated if the board operates beyond 10% load conditions for safety reasons.

   What is Skip mode? The NC1680 controller features a *Skip/Standby* mode which enables the application to achieve good no-load and light-load performance. In this mode the controller basically prevents the fast-leg switching for long periods of time to minimise the power consumption. During this time, with light load, the bulk capacitor discharges slowly; when it reaches certain voltage threshold the fast-leg switches again, charging up the bulk capacitor, and then the fast leg stops switching for another long period of time.
   The *Skip* mode can also be enabled by pulsing the PFCOK pin. The board provides placeholders to assemble the components to test the PFC_OK functionality following the NCP1680 datasheet recommendation, but this functionality has not been used or tested by CGD and is out of the scope of this user guide.

5. J4 - The evaluation board does not have a contactor to short the inrush NTC. Instead, there is a possibility to short the NTC by using J4. Shorting the NTC can be done ONLY if testing is carried out using an electronic ac source with peak current limit. All the testing carried out by CGD, and shown in this document have been done using an ac source and this is recommended. Shorting the NTC will improve the efficiency by not having the NTC resistance in the output path. Be aware that if the NTC is shorted and there is no other means to limit the inrush current like for example the ac source peak current limit, the operation is potentially unsafe and destructive.

6. R_{ZCD} physically separates GND and VOUT_RTN pins, and it is illustrated as R_{SENSE} in Figure 1. GND is considered the 0-V reference and VOUT_RTN corresponds to the negative terminal of the electrolytic capacitor in the output. Care must be taken to avoid shorting the R_{ZCD} resistor involuntary with the test equipment. For example, the ground leads of an Earth−connected oscilloscope probe must not be simultaneously connected to both GND and VOUT_RTN. This is particularly important if the user wants to measure with the oscilloscope the output voltage and other signals at the same time.

7. The circuit 0-V reference is physically separated, on the PCB layout, in two well differentiated sections:
   - GND, the control 0-V reference
   - PWRGND, the power 0-V reference.

   R35 and R43 (0 Ω resistors) mark the two single points on the PCB where GND and PWRGND are physically connected. The ground return paths for the power and control signals are separated to avoid power ground signals disturb low power control ground signals which can lead to related error signals in the controller.

8. The evaluation board includes a push button switch S2 to be able to discharge the bulk capacitors after power down.

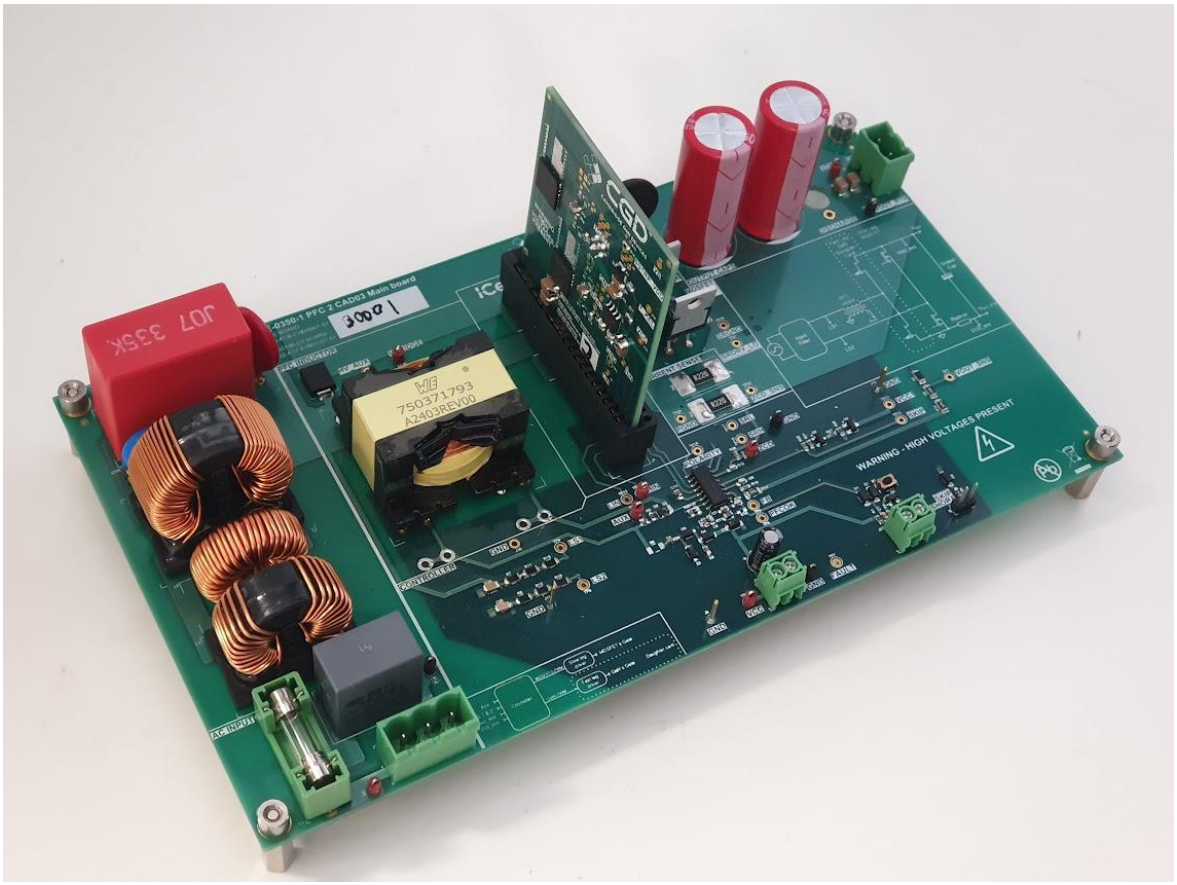


Figure 2 – 350 W TPPFC EVB. Daughterboard inserted in the mainboard in the correct position

3.1 Motherboard connectors and test points

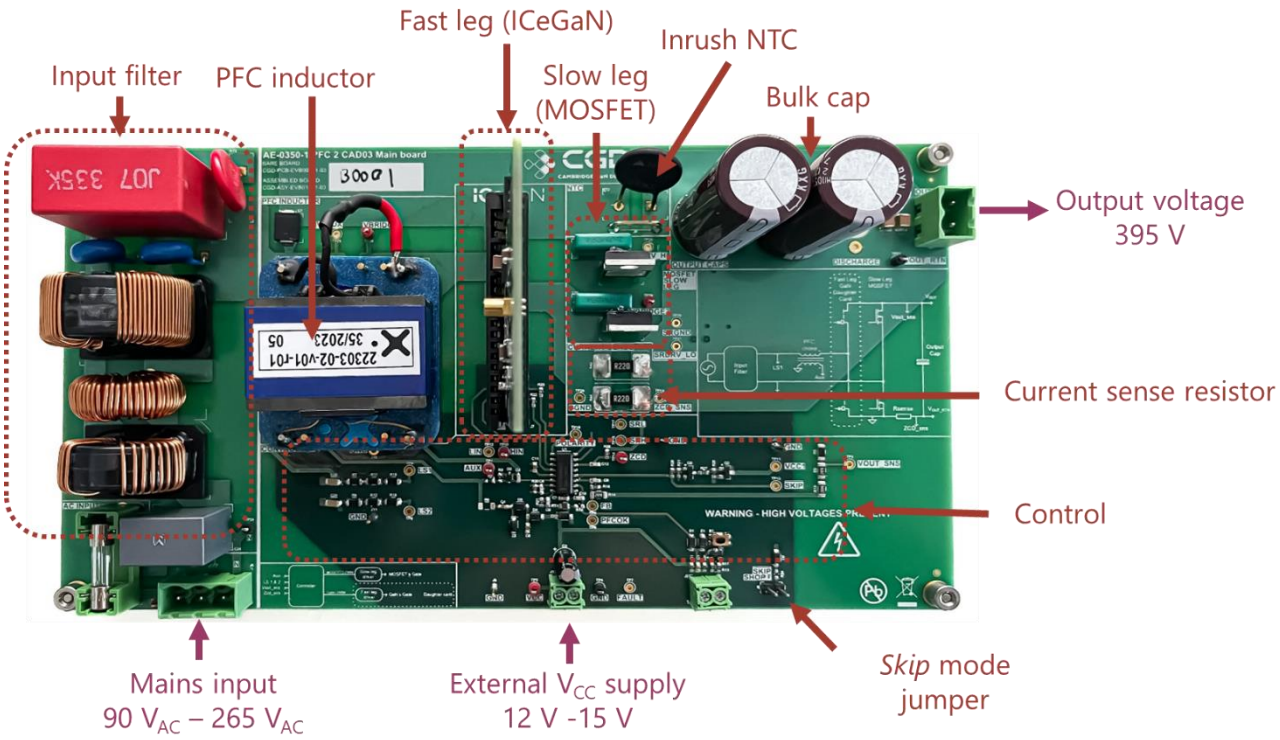


Figure 3 – Motherboard top view: main blocks and power connections

Table 2 – Motherboard I/O connectors

Connector	Function	Pinout	Description
J6	AC Input Voltage	1. AC Neutral 2. Earth 3. AC Line	90 V_{AC} / 265 V_{AC} input voltage
J5	DC Output Voltage	1. VOUT_RTN 2. VOUT	395 V_{DC} output voltage
J1	Low Voltage Rail	1. Vcc 2. GND	12 V / 15 V input voltage
J2	PFC_OK	1. Control Signal 2. GND	NOT USED. NCP1680 PFC_OK functionality
J3	Skip Mode	1. Control Signal 2. GND	OPEN for normal operation SHORTED for skip mode operation
J4	Inrush NTC Bypass	1. VOUT_NTC 2. VOUT	Jumper to short the inrush NTC. ONLY possible if there is an external current limit e.g. electronic AC Load.
J7	Daughterboard Interface	J7A. P1-P6 VOUT NTC J7B. P7-P12 VBRIDGE J7C. P13-P18 PWRGND J7D. S1-S5, S16-20 NOT CONNECTED J7D. S6, S7, S14, S15 GND J7D. S8, S13 GAN_LIN J7D. S9, S12 GAN_HIN J7D. S10, S11 VCC	Top Layer facing the PFC inductor

Table 3 – Motherboard test points

Motherboard Test Point	Signal	Description
J8, J9, J10 ,J11 , J12	GND	Control 0 V reference
TP1	AUX_L	PFC inductor auxiliary winding
TP2	VCC_IN	Vcc rail (12 V / 15 V)
TP3	VOUT_SNS	Output voltage
TP4	GND	Control 0 V reference near the NCP1680 PFC Controller
TP5	PCOK	Controller PFCOK pin
TP6	FB	Controller Feedback pin
TP7	FAULT	Controller Fault pin
TP8	LS1	Controller LVSNS1 pin / Line sense
TP9	LS2	Controller LVSNS2 pin / Line sense
TP10	PWMH	Controller PWM signal feeding the HB driver for the high side ICeGaN
TP11	VCC1	Voltage rail for the slow leg MOSFET driver. Disconnected in Skip Mode
TP12	PWML	Controller PWM signal feeding the HB driver for the low side ICeGaN
TP13	SKIP pin	Controller Skip pin
TP14	ZCD	Controller ZCD pin
TP15	SRH	Controller signal feeding the HB driver for the high side MOSFET
TP16	POLARITY	Controller pin for AC polarity
TP17	SRL	Controller signal feeding the HB driver for the low side MOSFET
TP18	ZCD_SNS	R_{ZCD} Voltage. Electrically same point as VOUT_RTN but closer to R_{ZCD}
TP19	SRGND	0 V control reference near the U2 (slow leg MOSFET driver)
TP20	SRDRV_HO	High side MOSFET gate
TP21	SRDRV_LO	Low side MOSFET gate
TP22	VOUT	Positive output voltage
TP23	VOUT_RTN	Negative output voltage (output 0V reference)
TP24	AC LINE	AC line
TP25	HV_AUX	PFC inductor pin 6
TP26	VBRDG	Slow leg (ICeGaN) Half bridge midpoint
TP27	AC NEUTRAL	AC neutral
TP28	VBRIDGE2	Slow leg (MOSFETs) Half bridge midpoint
TP29	PWRGND	Power 0 V reference

3.2 Daughterboard connectors and test points

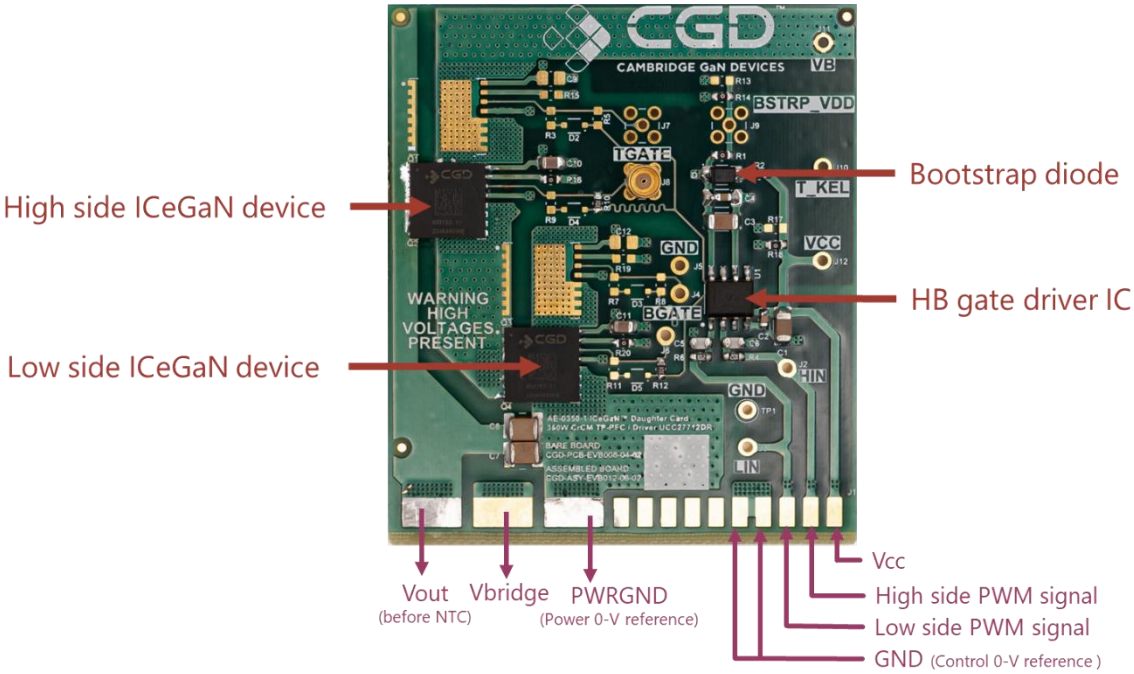


Figure 4 – Daughterboard top view

The daughterboard has been designed with the possibility to assemble ICeGaN devices in parallel in both the high side (HS), and the low side (LS) of the TPPFC fast-leg. However, ICeGaN parallel operation is out of the scope of this user guide, and all the test results present in this user guide were obtained with a single device on the HS and the LS, see Figure 4.

Table 4 – Daughterboard test points

Daughterboard Test Point	Signal	Description
TP3	HIN	High side PWM Driver input from the motherboard
TP5	LIN	Low side PWM Driver input from the motherboard
TP8	LS_GATE_1	Q3 gate
TP7	GND	Control 0 V reference
TP9	LS_GATE_2	Q4 gate
J7	Top_Gate_1 - Top Kelvin	MMCX connector. Q1 gate - Q1 kelvin
J8	Top_Gate_2 - Top_Kelvin	MMCX connector. Q2 gate - Q2 kelvin
J9	Bootstrap_VDD - Top_Kelvin	MMCX connector. Bootstrap line -Q1 kelvin
TP5	Top_Kelvin	High Side ICeGaN Kelvin connection
TP4	VB	Fast-leg (ICeGaN) Half bridge midpoint
TP2	VCC	Vcc line on the daughterboard
TP1	GND	Control 0 V reference

3.3 Test set up arrangement

The bench test set up to obtain the test results presented in this user guide, is described below:

- For efficiency measurements where output power was equal or higher than 10% load, one power meter was attached to the input to measure input power, power factor and THD and a second power meter was connected to the output to measure output power. Efficiency was calculated using the power measurements. Figure 5 illustrates how the power meters were arranged. The voltmeter in the input was connected directly to test points, TP24 and TP27. The voltmeter in the output was connected directly to test points, TP22 and TP23.

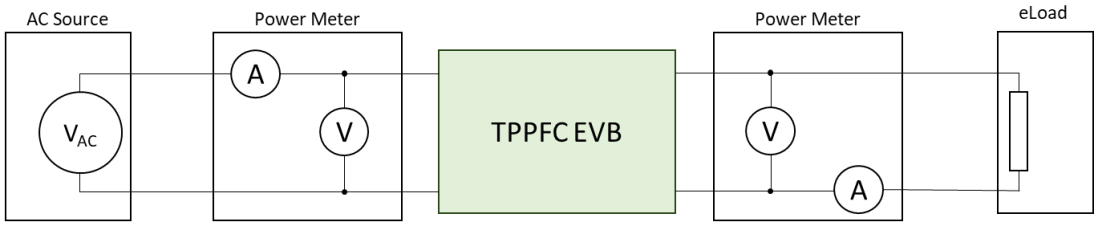


Figure 5 – Test set up for efficiency measurements

- Figure 6 illustrates the arrangement to measure no load power.

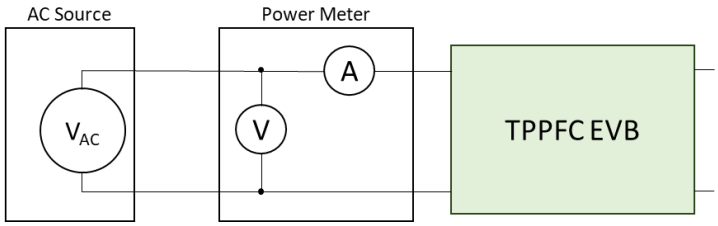


Figure 6 - Test set up for no load power measurements

In both cases 12V was supplied to the low voltage rail in J1.

4 Test Results

All the results shown in this section have been obtained powering the board with an electronic ac source and using an electronic load.

4.1 Efficiency

Table 5 – Efficiency results

CGD 350 W TPPFC EVB Efficiency						
	10% Load	**25% Load**	**50% Load**	**75% Load**	**100% Load**	**Average**
90 V_{AC}	97.09%	97.39%	97.42%	96.84%	95.88%	96.88%
115 V_{AC}	97.26%	97.76%	97.75%	97.75%	97.33%	97.65%
230 V_{AC}	97.24%	98.59%	98.75%	98.73%	98.76%	98.71%
265 V_{AC}	97.86%	98.67%	98.98%	98.99%	98.98%	98.91%

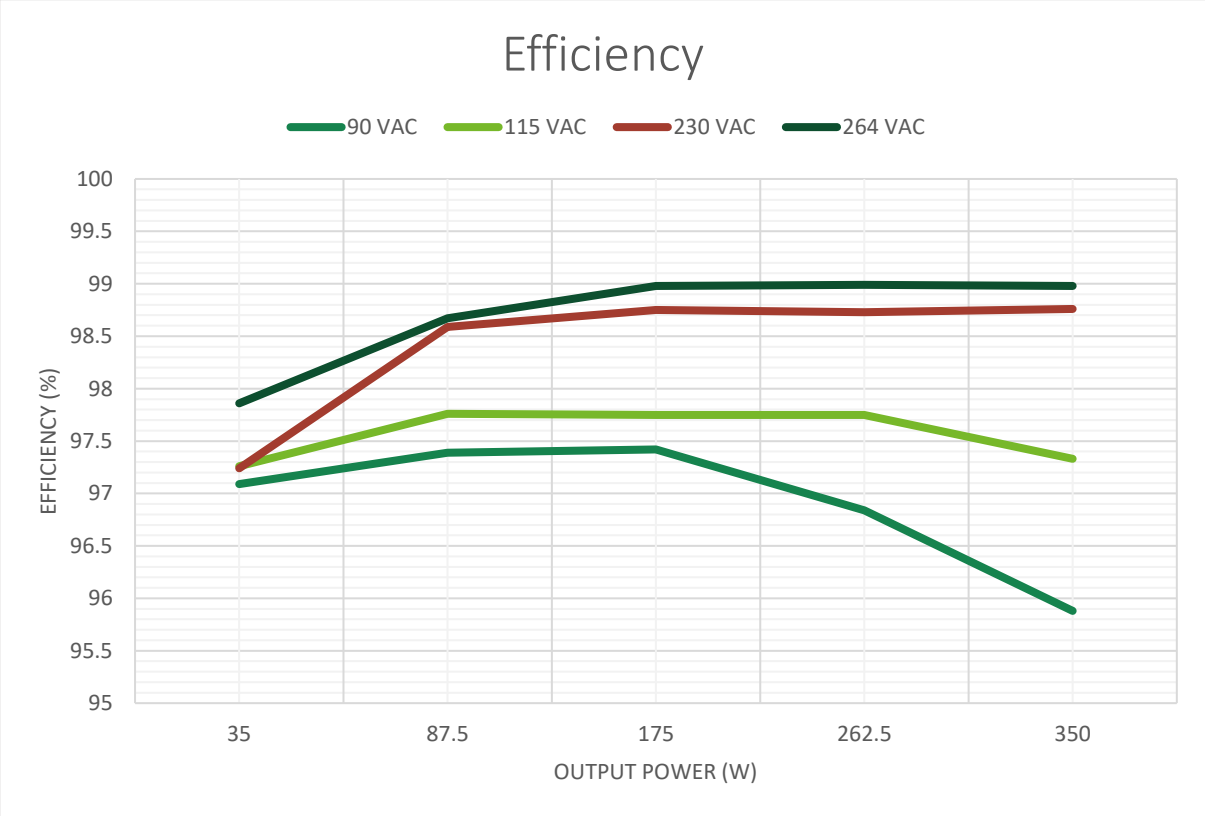


Figure 7 – Efficiency curves at 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} input voltage

Note: *The input power and the output power were measured using a GW Instek GPM-8320 power meter. Electronic load: Chroma 63600-2: AC voltage Source: IT7803.*

4.2 No load power

Table 6 – No load power

CGD 350 W TPPFC EVB No load Power	
90 V_{AC}	30 mW
115 V_{AC}	34 mW
230 V_{AC}	77 mW
265 V_{AC}	90 mW

Notes:

1. *For the no load power measurement, the load was physically disconnected*
2. *The no load power was obtained employing a GW Instek GPM-8310 power meter integration feature for more than 20 minutes. The power meter was wired as illustrated in Figure 6.*
3. *The AC source used in this test was the APS-7050*
4. *The NCP1680 TPPFC skip mode operation was externally activated shorting the J3 jumper.*

4.3 Power factor (PF) and total harmonic distortion (THD)

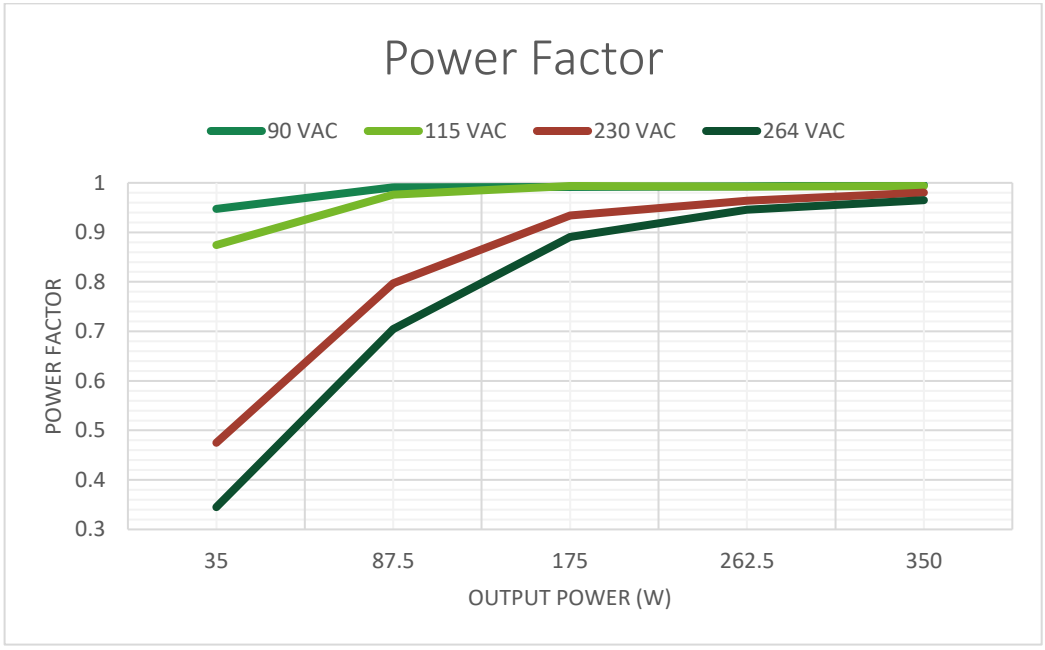


Figure 8 – Power factor vs load

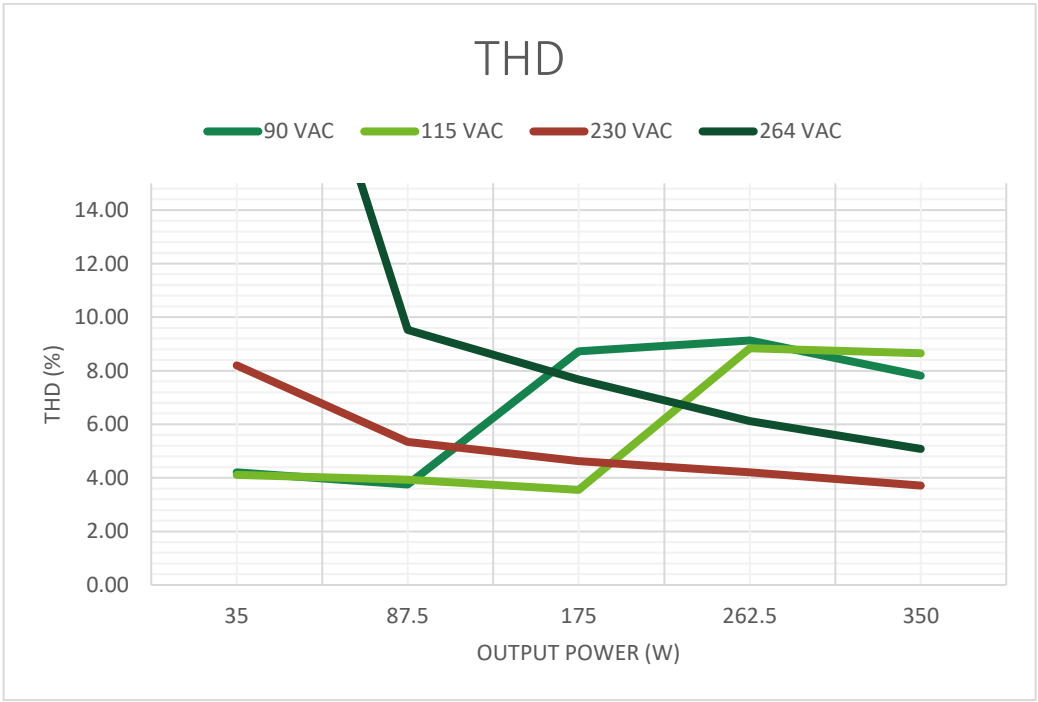


Figure 9 – THD vs load

5 Design Considerations

In a CrCM TPPFC topology, the inductor current resets back to zero, and low reverse recovery charge (Q_{RR}) Si MOSFETs could be used in the fast leg. However, ICeGaN devices offer a better choice to increase efficiency and have less thermal stress. ICeGaN is a GaN HEMT device; has no Q_{RR}, Q_G is approximately 10 times less than in a MOSFET with the same $R_{DS(on)}$ and C_{OSS} is also lower and more linear. As a result, switching losses are insignificant when using ICeGaN in a CrCM TPPFC.

Unlike other GaN HEMT alternatives, ICeGaN is very simple to drive. There is no need for negative drive or any additional requirements to use a special gate driver. Therefore, a standard MOSFET HB gate driver is employed in this EVB. Each ICeGaN only requires two small SMD components; a capacitor between V_{DD} and Kelvin pins, and an external gate resistor. The V_{DD} voltage of the low and high ICeGaN is taken from Vcc and bootstrap rail voltages of the gate-driver IC.

ICeGaN gate drive voltage range is 9 V to 20 V, allowing a broad gate-driver IC selection. A traditional MOSFET HB gate driver is used instead of a dedicated GaN gate-driver IC. The external gate drive voltage is clamped to the optimum level on the internal gate of the ICeGaN device. This extends lifetime and reliability.

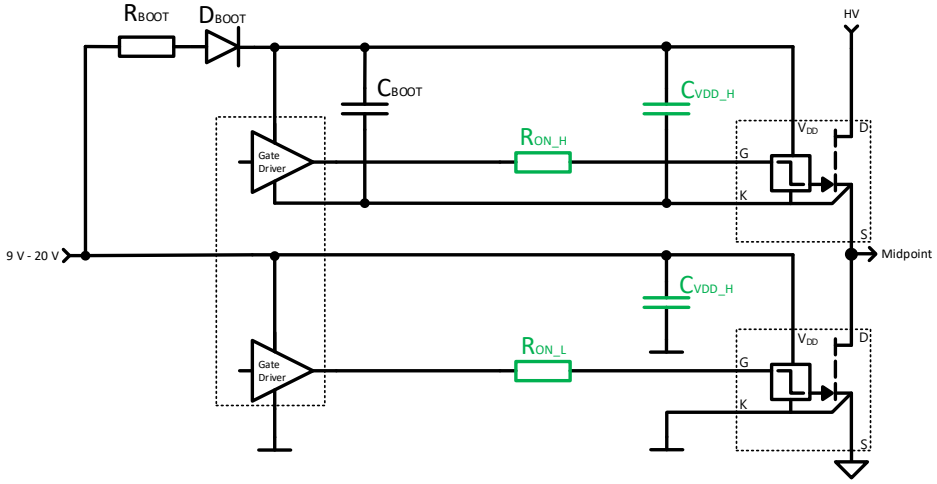


Figure 10 – External SMD components (in green) needed to drive ICeGaN with a bootstrap HB gate driver

The ICeGaN internal Miller Clamp is a major advantage over other GaN HEMTs. The internal Miller Clamp operates when V_{DD} is present, and clamps the internal gate voltage to zero volts. This means that the vast majority of the Miller current generated by the V_{DS} dv/dt does not flow through external gate resistor. Therefore, parasitic inductance on the gate path is almost irrelevant at turn off, and undesirable spurious turn-on events are easily avoided. As a result, there is no need for negative gate drive, and there is no need for an external gate turn-off path. Thanks to the low gate charge, 4 nC in CGD65A055SH2, gate switching losses are negligible, and the gate driver does not required as much sink and source current capability compared with the use of a MOSFET. This EVB uses 20 Ω turn-on gate resistors in each ICeGaN device, and PCB layout on the gate paths are not as critical as with conventional GaN HEMT alternatives.

When the ICeGaN devices are not switching, the current flowing into their V_{DD} pin is almost zero. The ICeGaN V_{DD} pin only draws 1.6 mA when the gate pin voltage is in on state and maximum 150 µA when the gate pin voltage is in off state; this feature was implemented to reduce power consumption under no-load conditions. In addition, when the EVB operates in

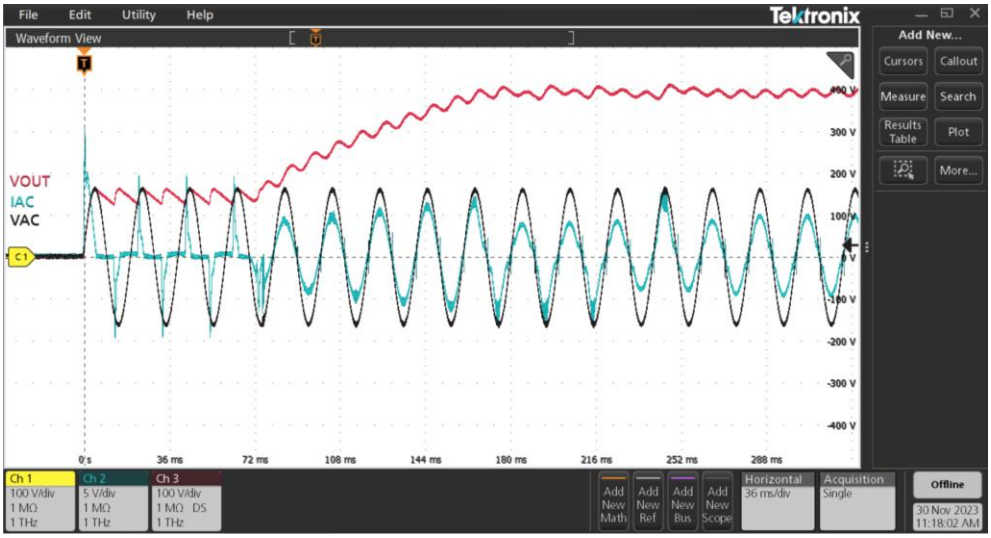
no-load operation, and the HS ICeGaN device is not switching the bootstrap voltage rail does not get depleted by the current flowing into the V_{DD} pin. That ensures the high-side driver never goes into under voltage lock-out (UVLO).

In summary, compared to MOSFETS or discrete GaN devices, ICeGaN 55 mΩ device is an excellent choice for a CrCM TPPFC for two main reasons,:

1. ICeGaN is an IC based on e-GaN HEMT device. Therefore switching losses are negligible in this topology, which boost efficiency and power density and minimize no load power consumption.
2. Driving ICeGaN devices is very simple and cost effective. Only a standard HB driver and four SMD components are required, See Figure 10.

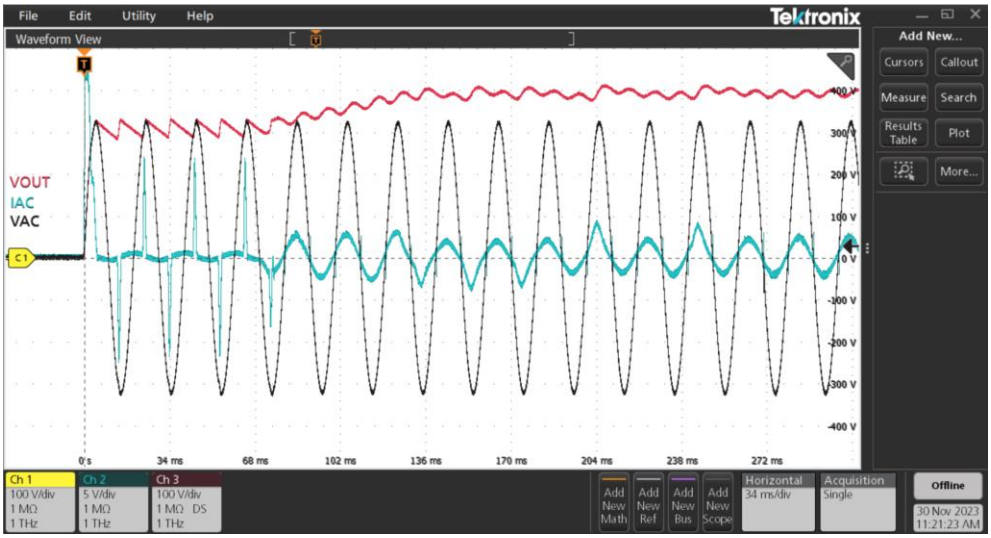
6 Waveforms

6.1 Start-up at full load waveforms



CH 1 – Input voltage CH 2 – Input current (Amps) CH 3 – Output voltage

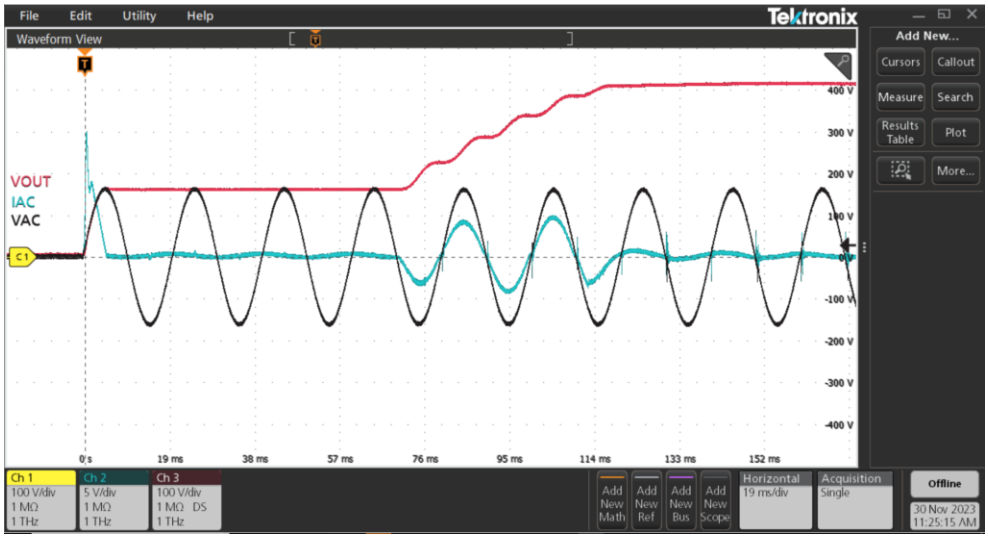
Figure 11 – Start-up at 115 V_{AC} / 350 W



CH 1 – Input voltage CH 2 – Input current (Amps) CH 3 – Output voltage

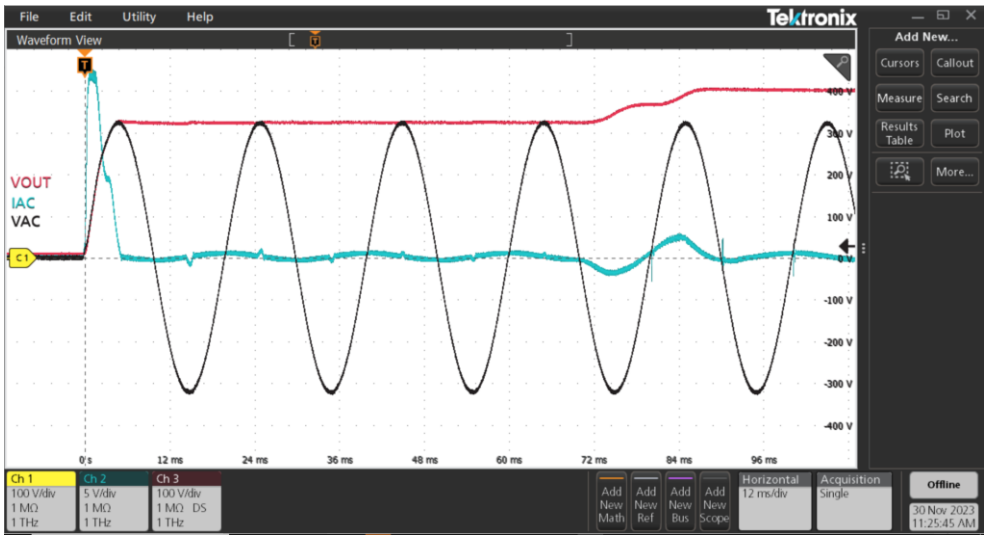
Figure 12 – Start-up at 230 V_{AC} / 350 W

6.2 Start-up at no-load waveforms



CH 1 – Input voltage CH 2 – Input current (Amps) CH 3 – Output voltage

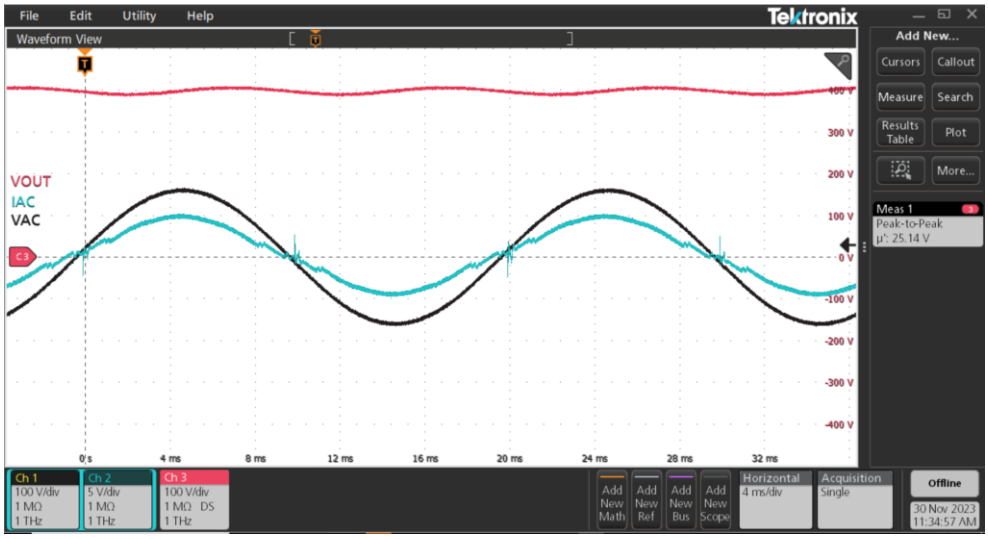
Figure13 – Start-up at 115 V_{AC} / no load



CH 1 – Input voltage CH 2 – Input current (Amps) CH 3 – Output voltage

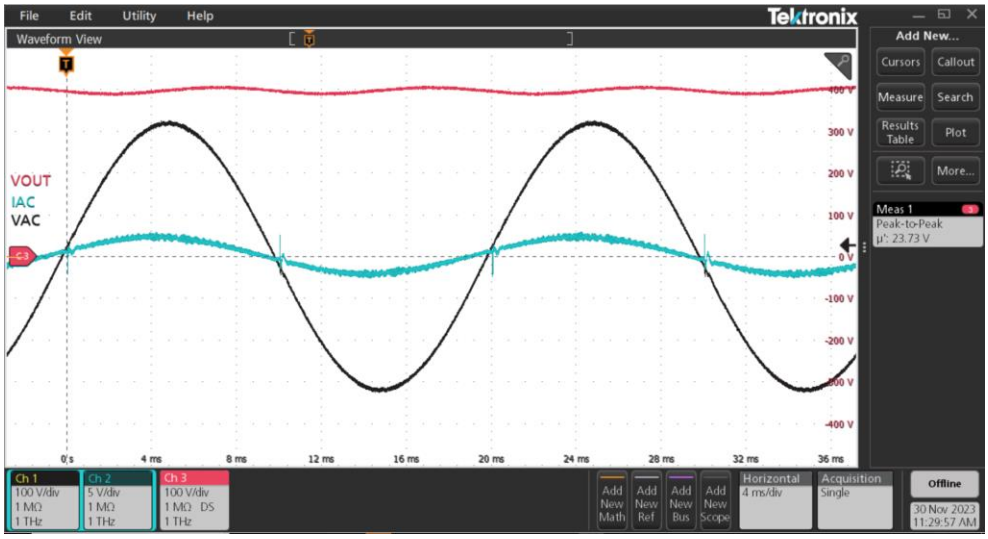
Figure 14 – Start-up at 230 V_{AC} / no load

6.3 Steady state waveforms



CH 1 – Input voltage CH 2 – Input current (Amps) CH 3 – Output voltage

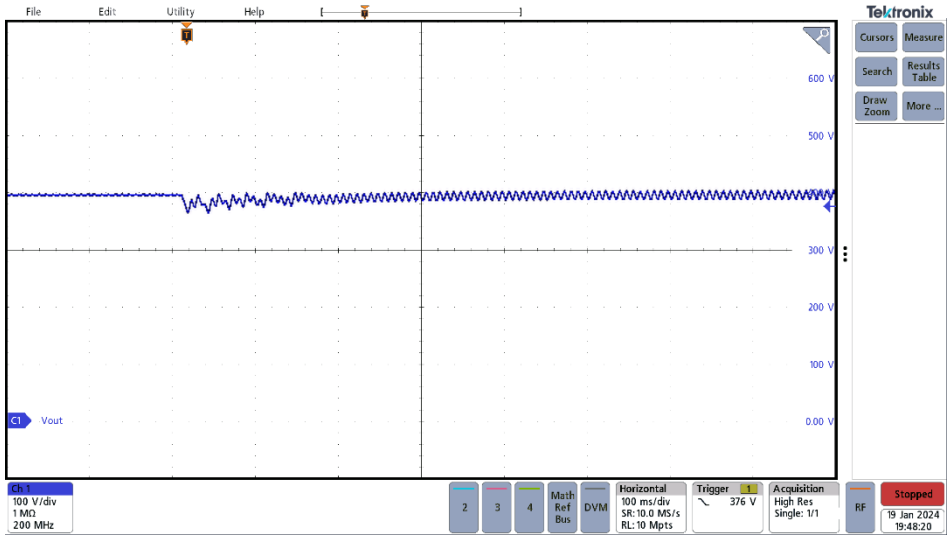
Figure 15 – Input current and output voltage at 115 V_{AC} / 350 W



CH 1 – Input voltage CH 2 – Input current (Amps) CH 3 – Output voltage

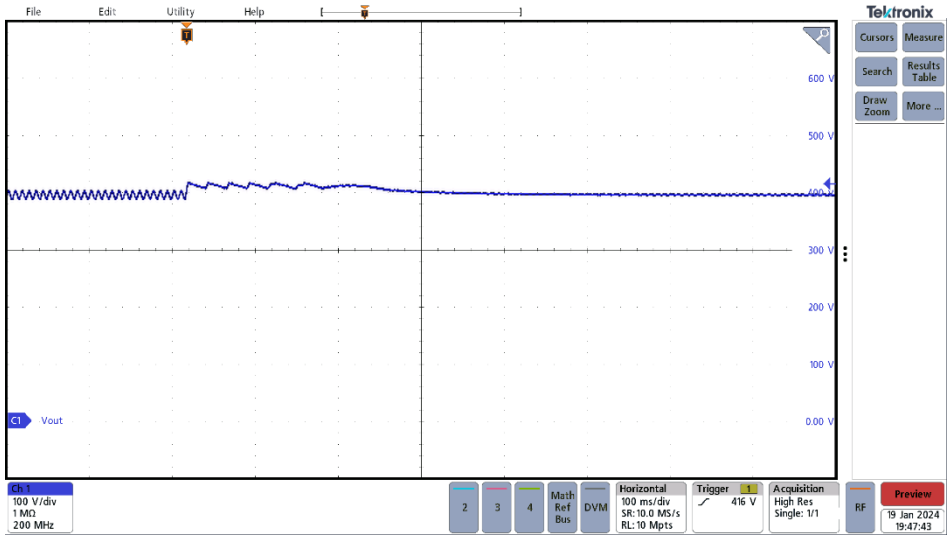
Figure 16 – Input current and output voltage at 230 V_{AC} / 350 W

6.4 Load step response



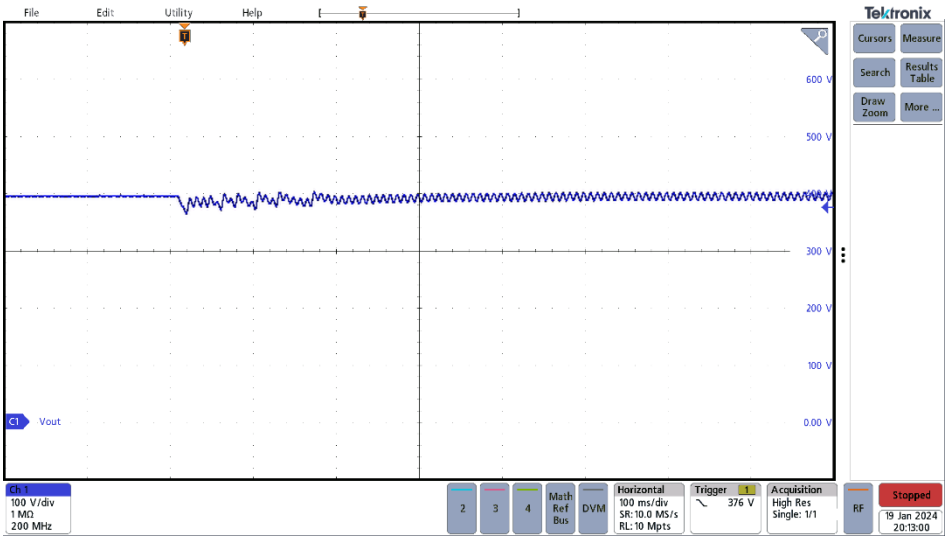
CH 1 – Input current (Amps) CH 2 – Fast-leg midpoint voltage CH 3 – Output voltage

Figure 17 – 10% to 100% step load at 115 V_{AC}



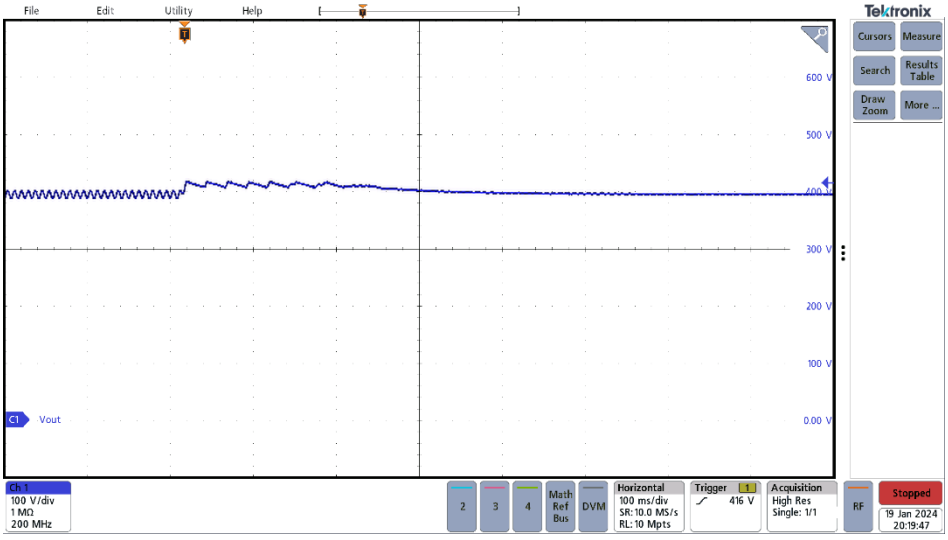
CH 1 – Input current (Amps) CH 2 – Fast-leg midpoint voltage CH 3 – Output voltage

Figure 18 – 100% to 10% step load at 115 V_{AC}



CH 1 – Input current (Amps) CH 2 – Fast-leg midpoint voltage CH 3 – Output voltage

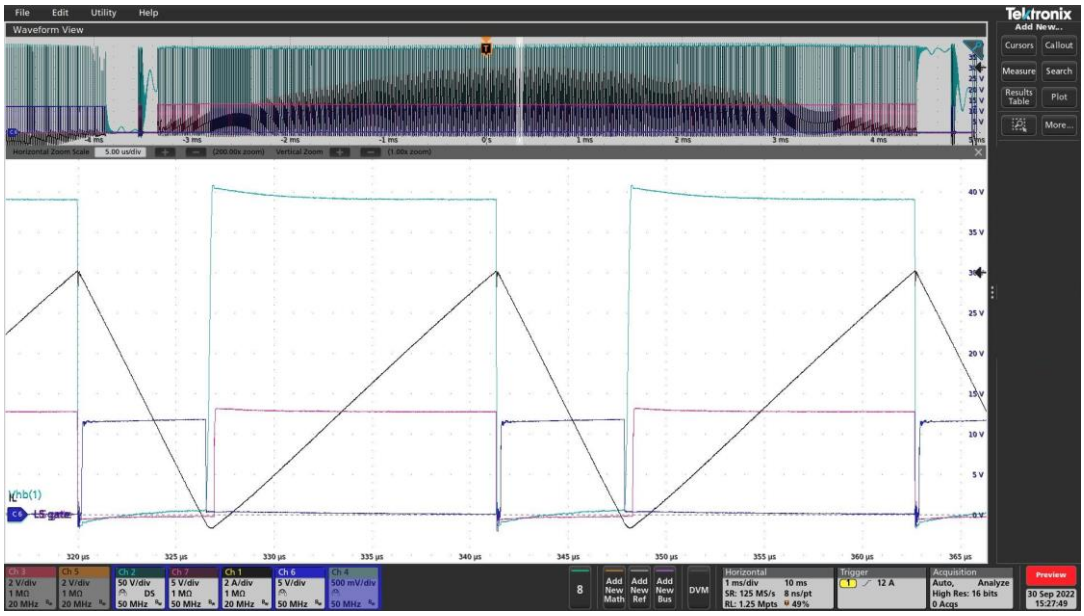
Figure 19 – 10% to 100% step load at 230 V_{AC}



CH 1 – Input current (Amps) CH 2 – Fast-leg midpoint voltage CH 3 – Output voltage

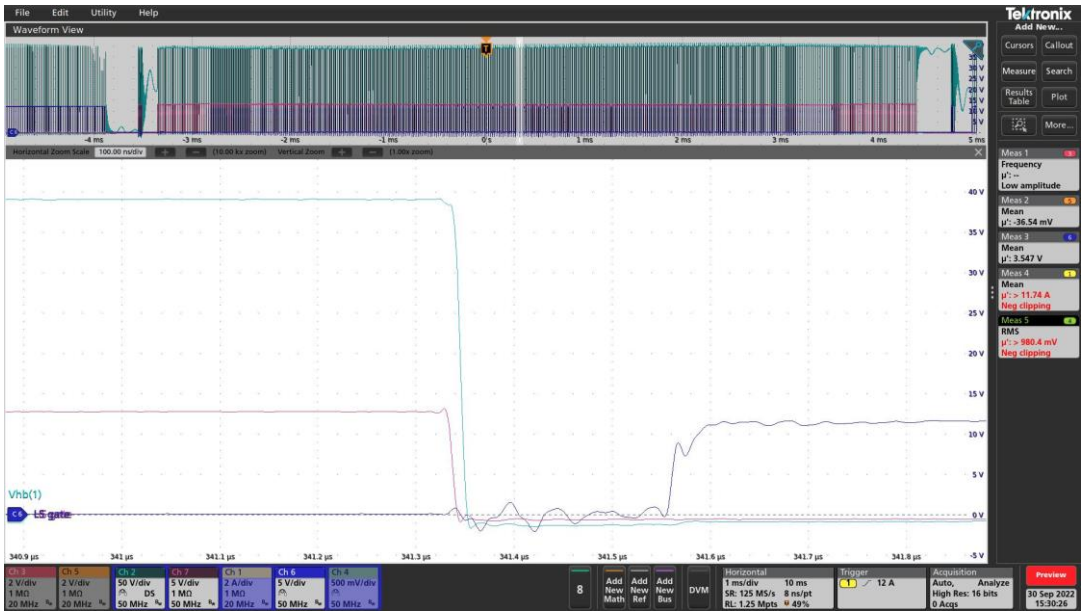
Figure 20 – 100% to 10% step load at 230 V_{AC}

6.5 TPPFC ICeGaN switching operation



CH 1 – PFC inductor current | CH 2 – PFC fast-leg midpoint voltage | CH 7 – HS ICeGaN gate voltage | CH 6 – LS ICeGaN gate voltage

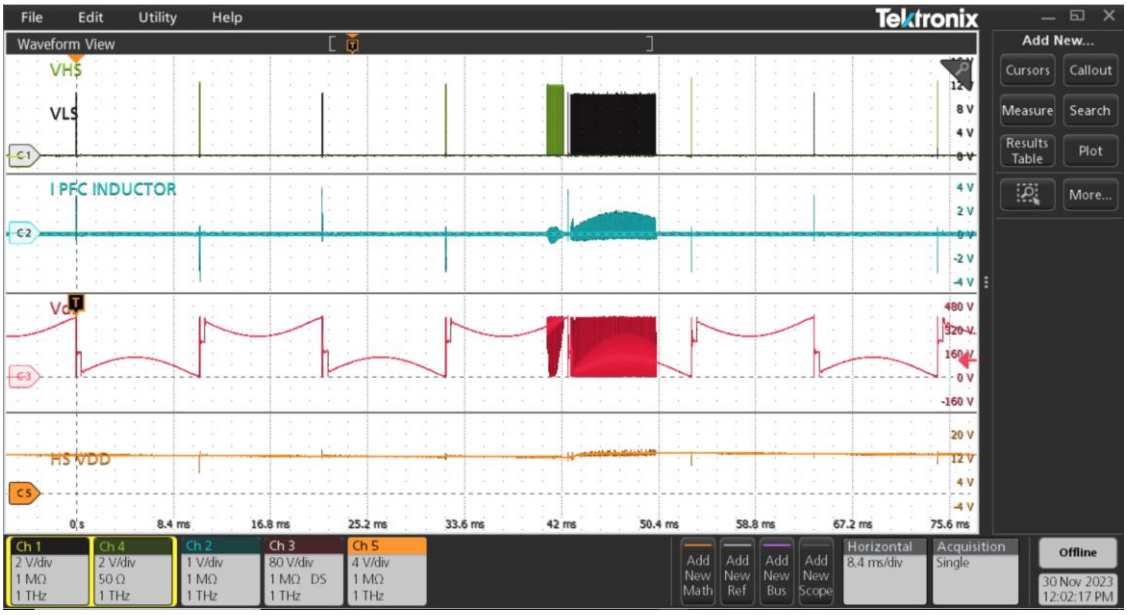
Figure 21 – ICeGaN TPPFC switching waveforms at 90 V_{AC} / 340 W (during an AC negative cycle)



CH 1 – PFC inductor current | CH 2 – PFC fast-leg midpoint voltage | CH 7 – HS ICeGaN gate voltage | CH 6 – LS ICeGaN gate voltage

Figure 22 – High side ICeGaN turn-off (during an ac negative cycle)

6.6 Bootstrap voltage and ICeGaN V_{DD} during no load



CH 1 – Low side ICeGaN V_{GS} | CH 2 – PFC inductor current (Amps) | CH 3 – Fast-leg midpoint voltage | CH 4– High side ICeGaN V_{GS} | CH 5– Bootstrap voltage

Figure 23 – Bootstrap voltage at 90 V_{AC} / no load

Figure 23 shows the low consumption of ICeGaN V_{DD} pin during off state. The V_{DD} pin maximum off-state current is 150 µA. For this reason, the bootstrap voltage rail stays almost at the same voltage level avoiding issues with the driver UVLO even during long periods.

7 Thermal Results

The daughterboard PCB was designed to allocate four ICeGaN devices to allow parallel operation. As previously mentioned, ICeGaN parallel operation is out of the scope of this user guide, and only single devices are assembled on the board. The extra copper of the non-fitted parts effectively act as a heat spreader. As a result, the daughterboard does not need an additional metal heatsink or additional air flow to operate.

The high side ICeGaN device temperature is 82 ºC when the unit reaches thermal stability after running 40 minutes under the more stringent operating conditions (90 V_{AC} / 350 W). This is shown below in Figure 24.

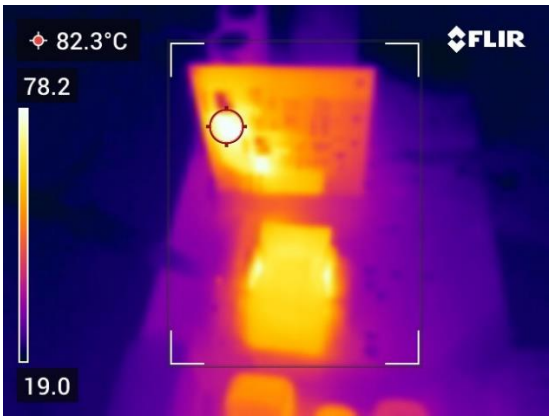


Figure 24 - Fast-leg high-side ICeGaN temperature after 40 min at 90 V_{AC} / 350 W

The temperature of ICeGaN device is 63 ºC at 115 V_{AC} and 45 ºC at 230 V_{AC}, operating at 350 W, when thermal stability is reached. This is shown in Figure 25 and Figure 26 respectively.

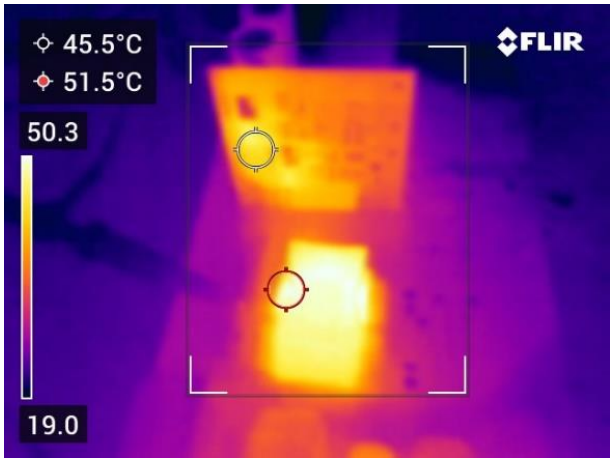


Figure 25 - Fast-leg high-side ICeGaN temperature after 40 min at 115 V_{AC} / 350 W

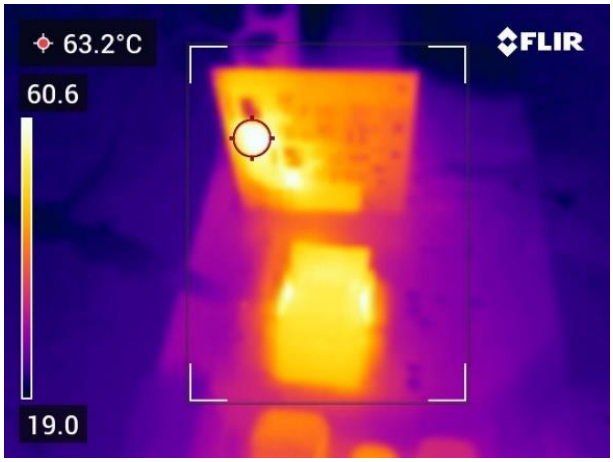


Figure 26 - Fast-leg high-side ICeGaN temperature after 40 min at 230 V_{AC} / 350 W

.

8 Schematic

8.1 Motherboard

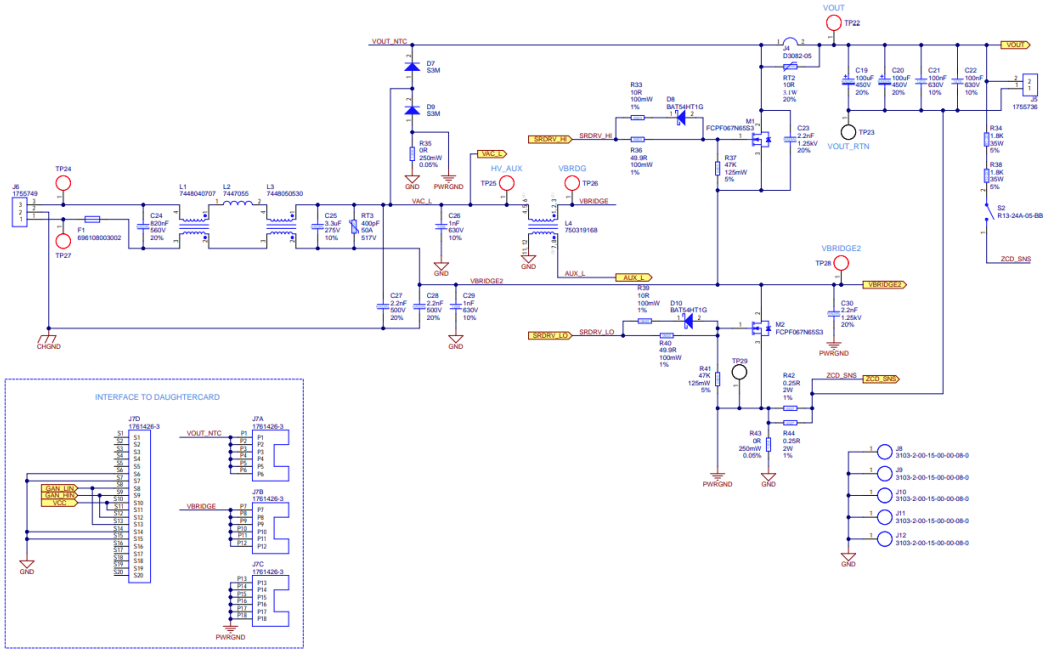


Figure 27 – Motherboard power section schematic

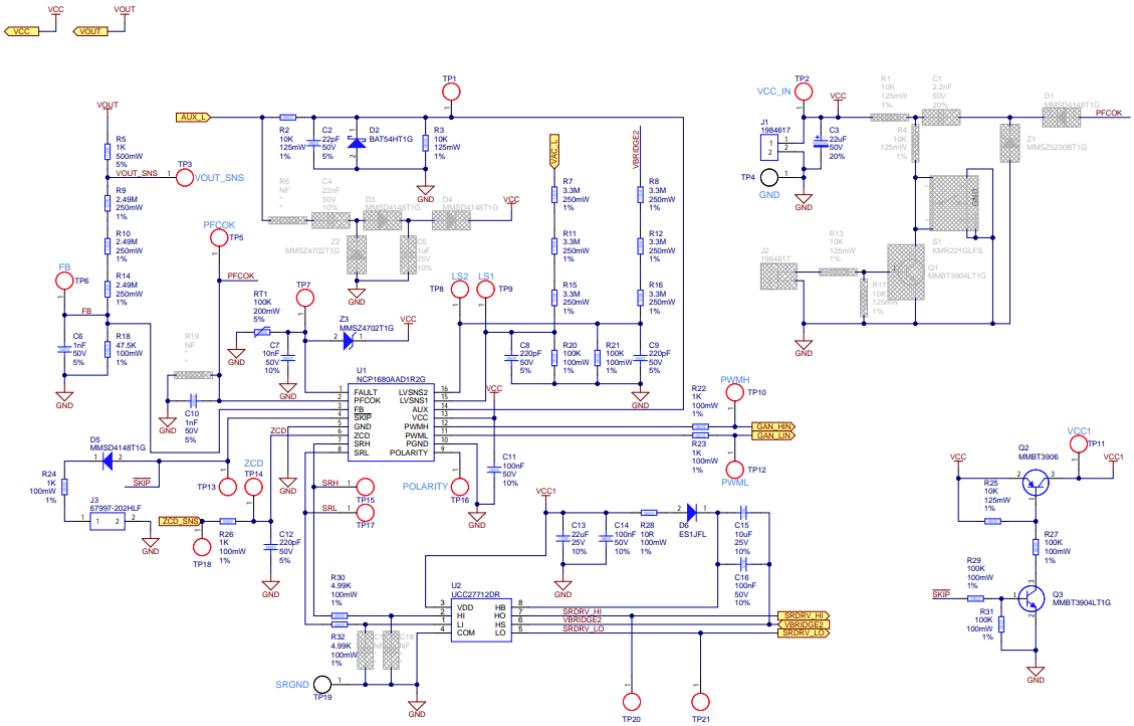


Figure 28 – Motherboard control section schematic

8.2 TPPFC fast-leg ICeGaN daughterboard schematic

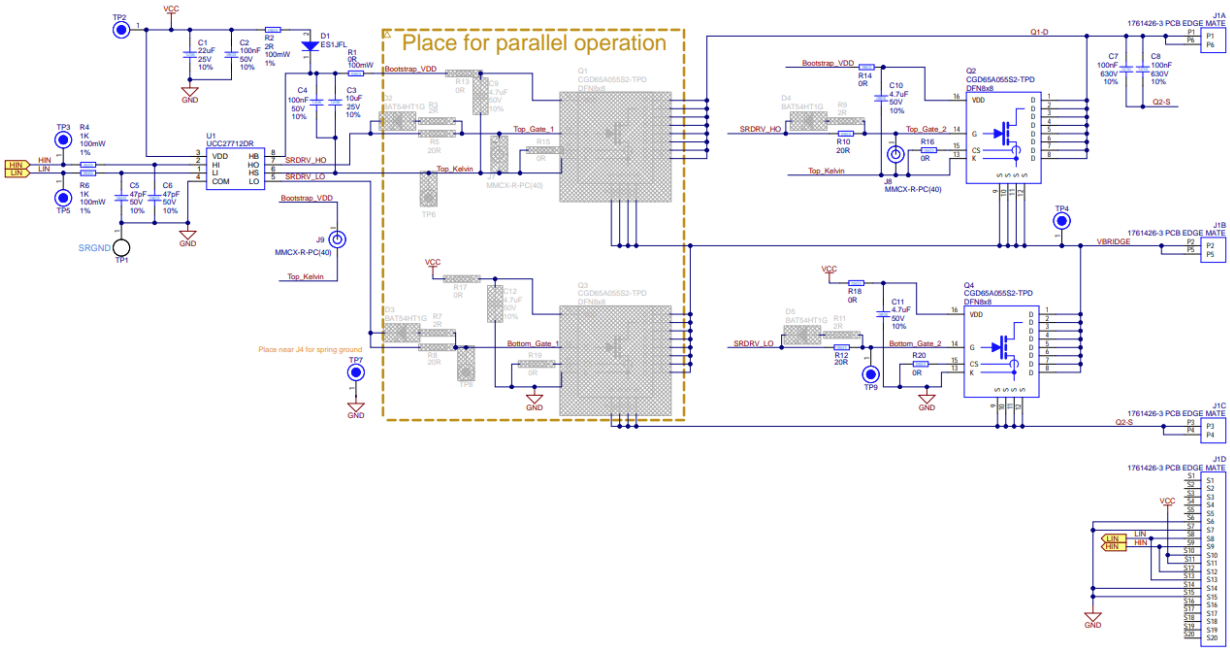


Figure 29 – Daughterboard schematic

9 PCB Layout

9.1 Motherboard layout

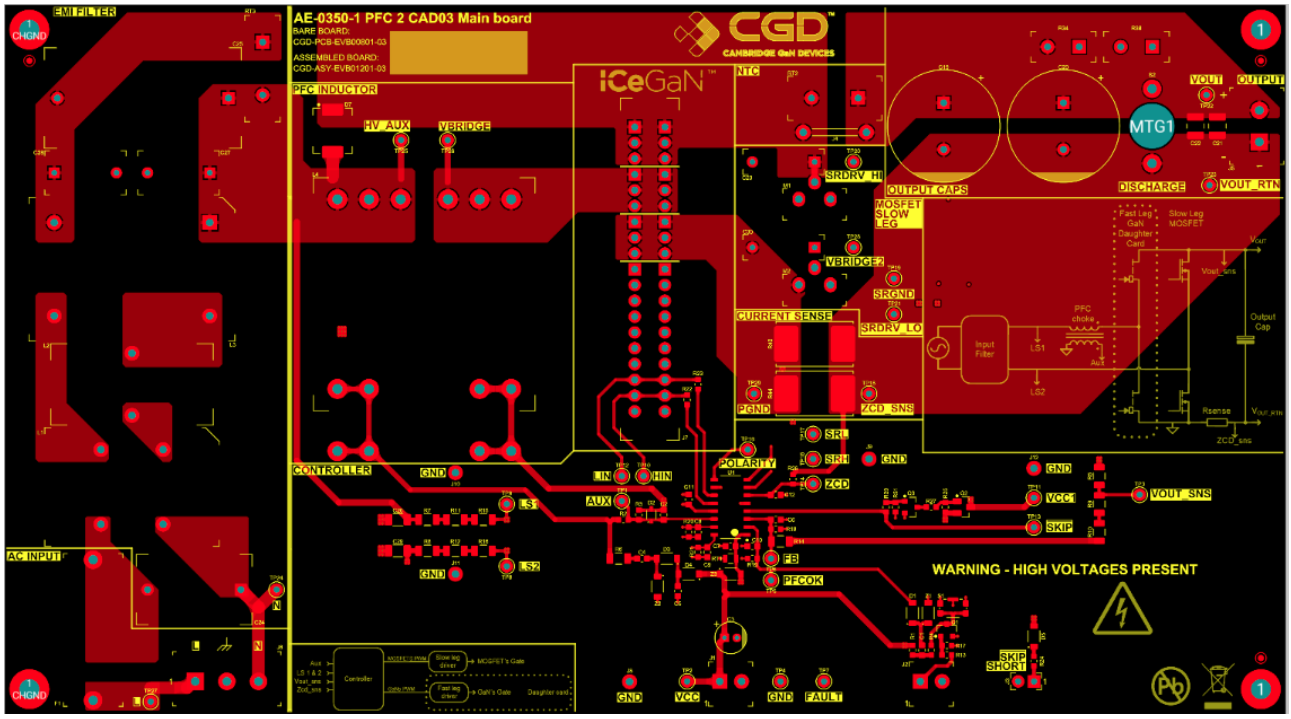


Figure 30 – Motherboard layout: top layer

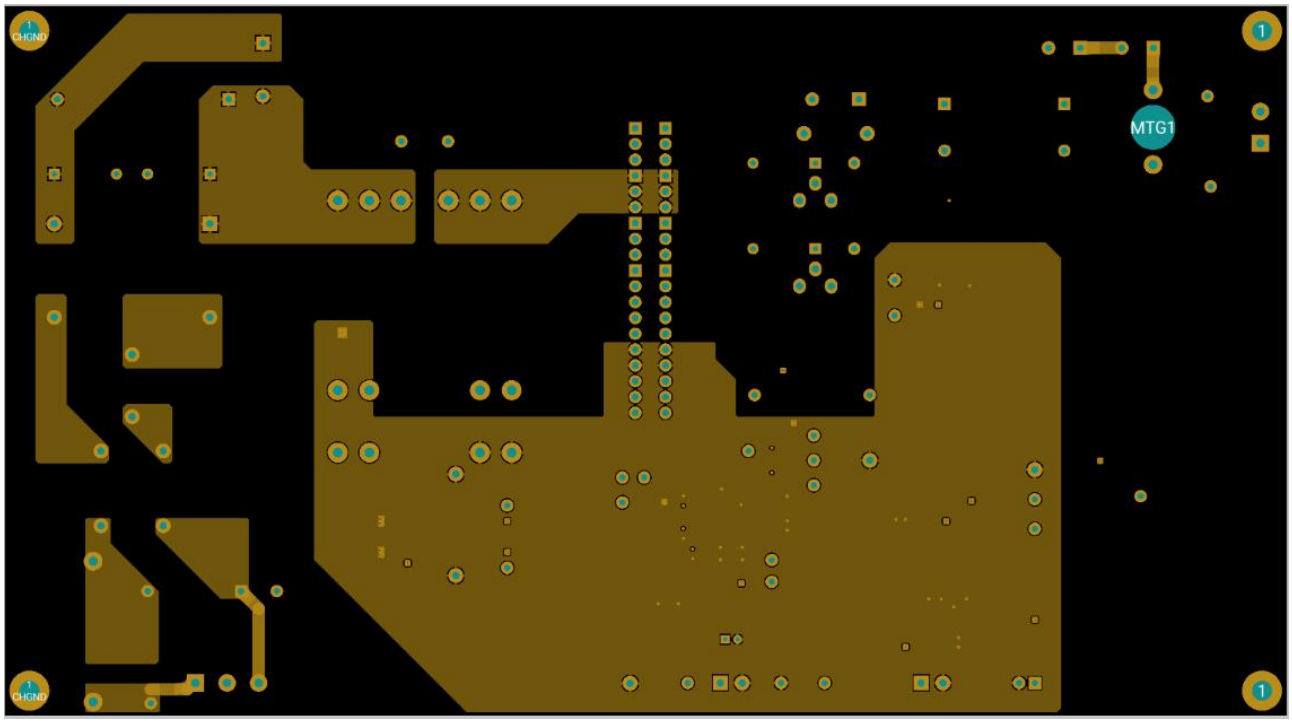


Figure 31 – Motherboard layout: inner layer 1

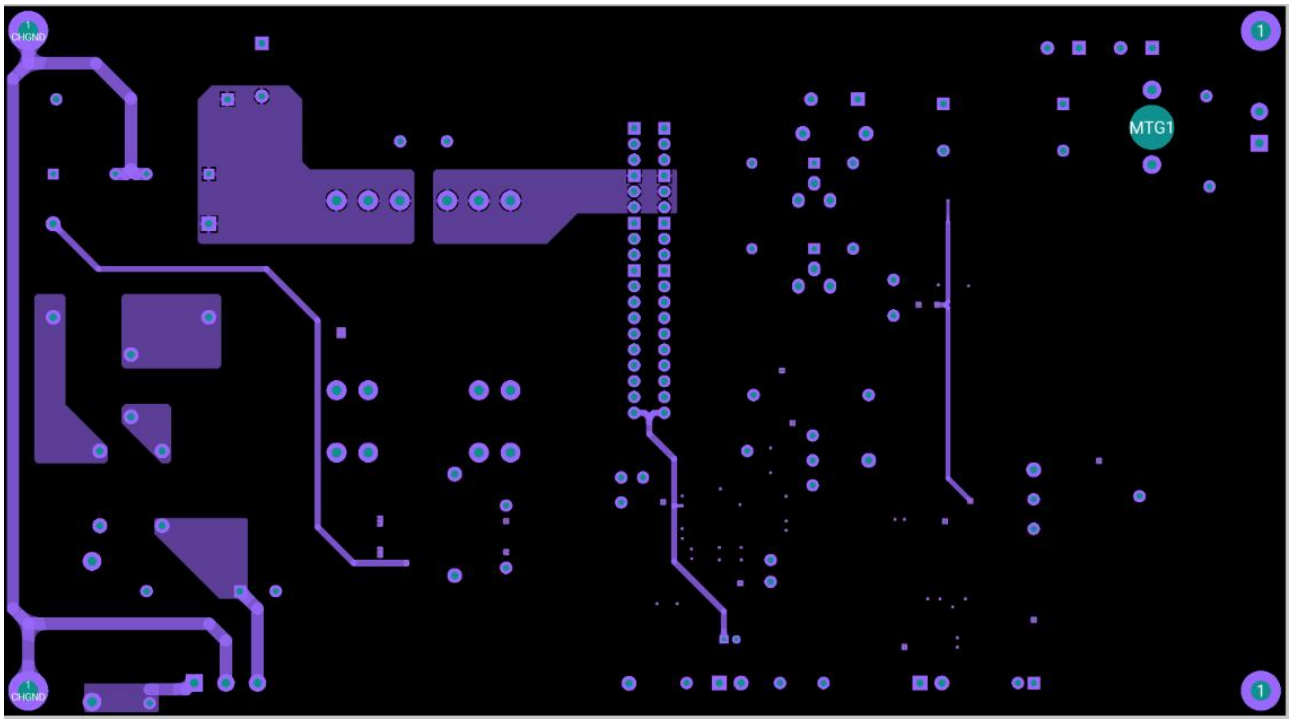


Figure 32 – Motherboard layout: inner layer 2

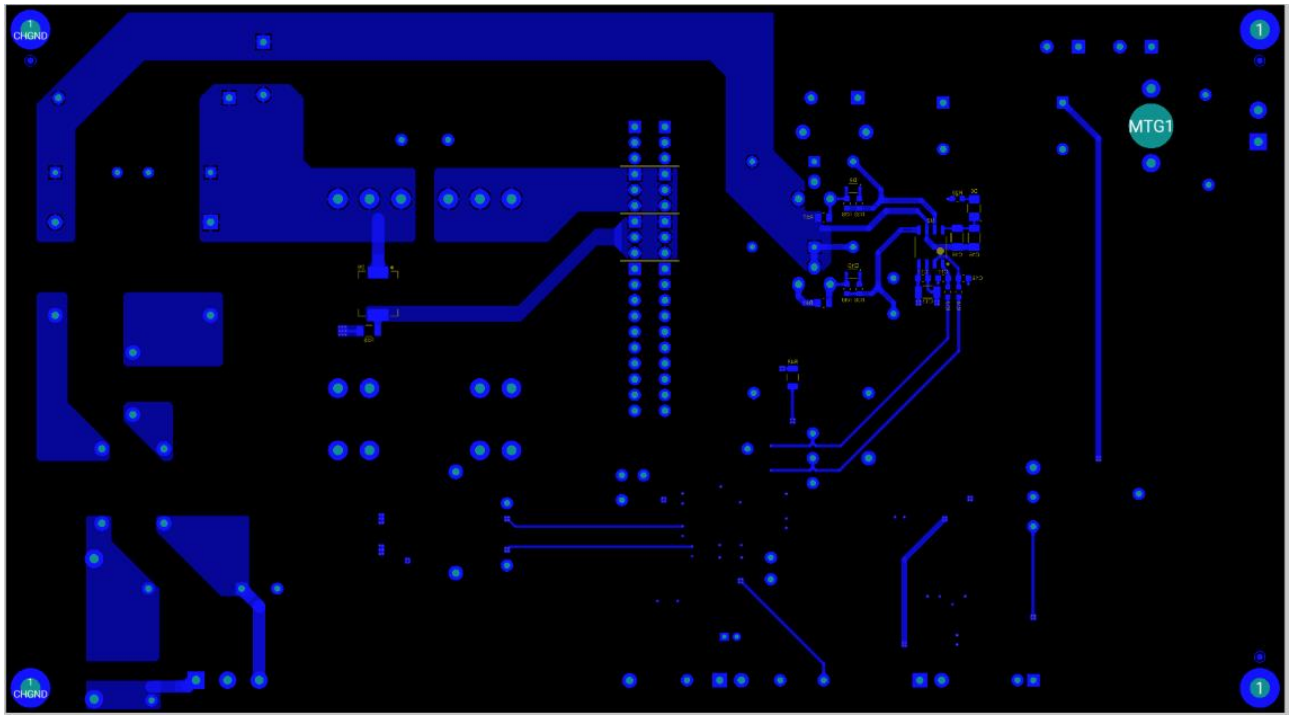


Figure 33 – Motherboard layout: bottom layer

9.2 Daughterboard layout

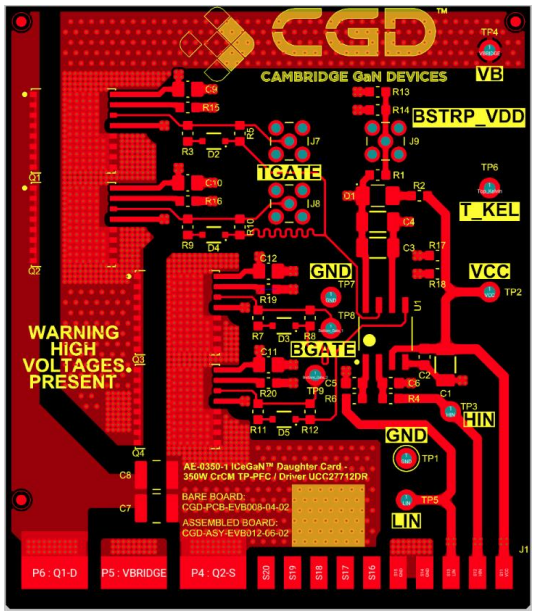


Figure 34 – Daughterboard layout: top layer

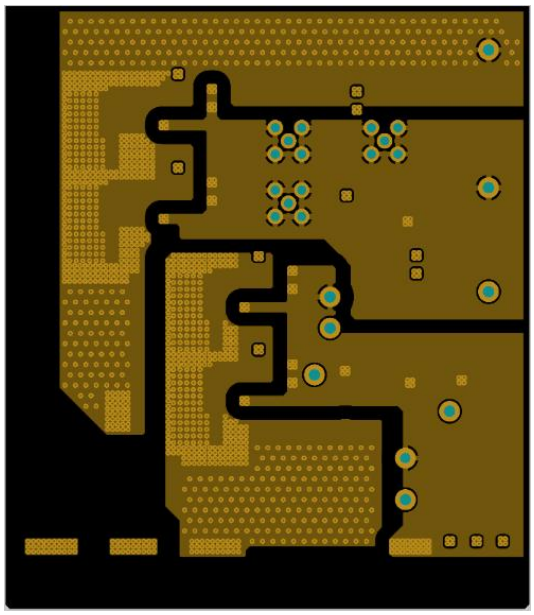


Figure 35 – Daughterboard layout: inner layer 1

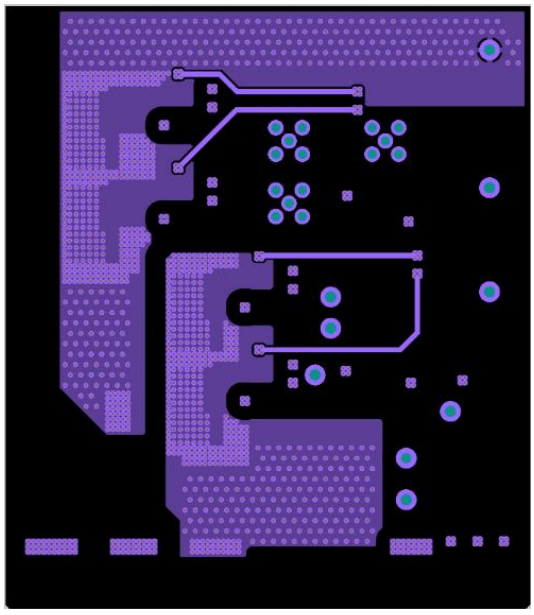


Figure 36 – Daughterboard layout: inner layer 2

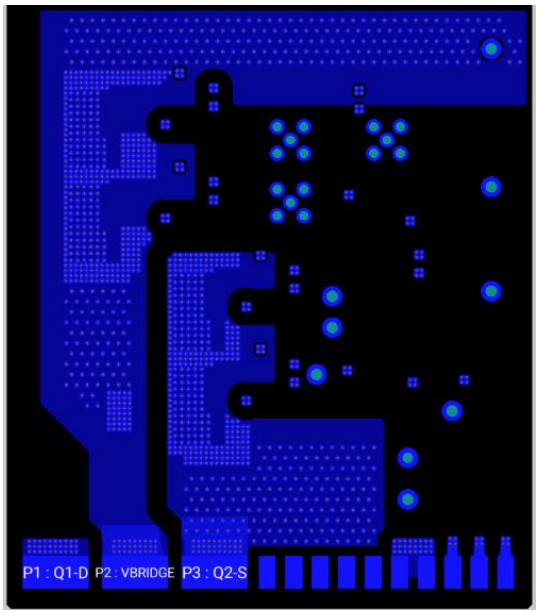


Figure 37 – Daughterboard layout: bottom layer

11 PFC Inductor datasheets

CGD's 350W TPPFC EVB can operate with two different PFC inductor versions. Although the designs are slightly different and use different core geometries, the electrical characteristics are the same and there is no real difference in terms of efficiency or thermal operation. Below are the datasheets of both versions:

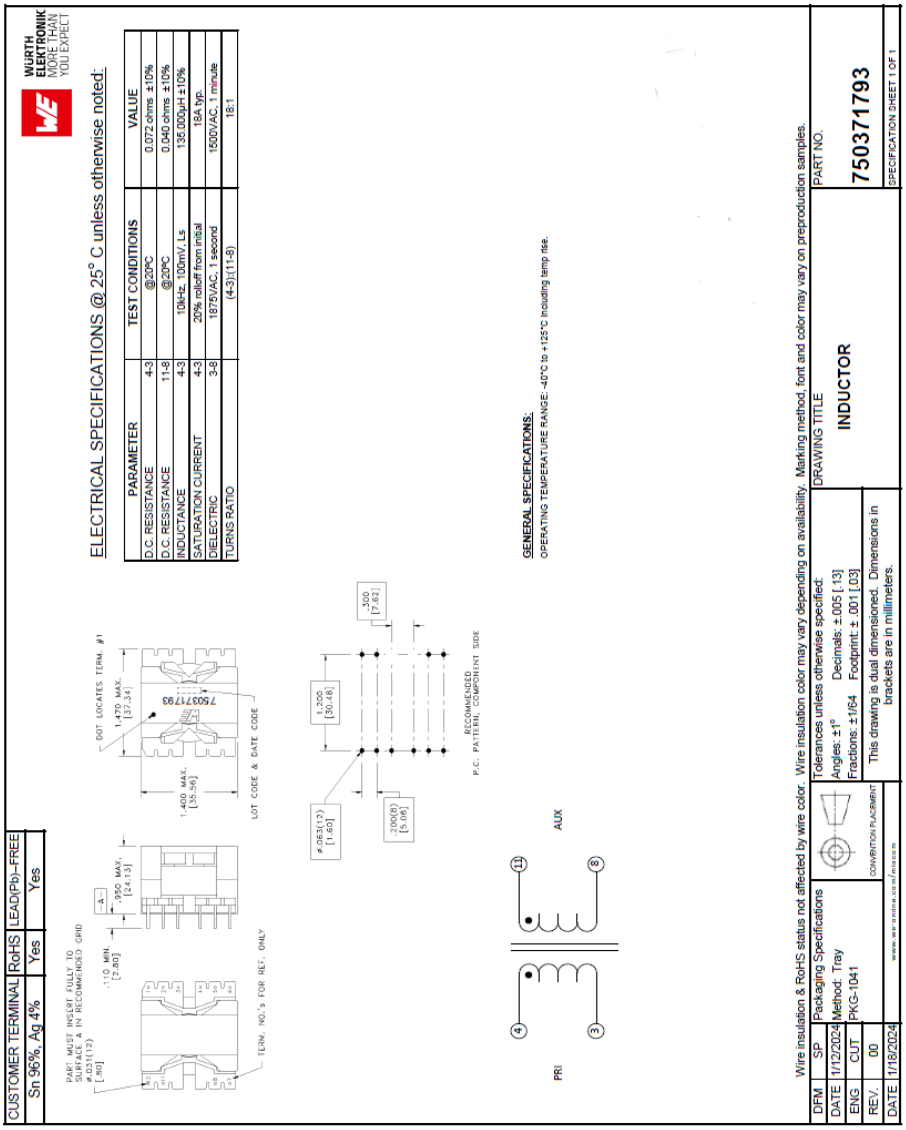


Figure 38 – Wurth PFC inductor 750371793 datasheet

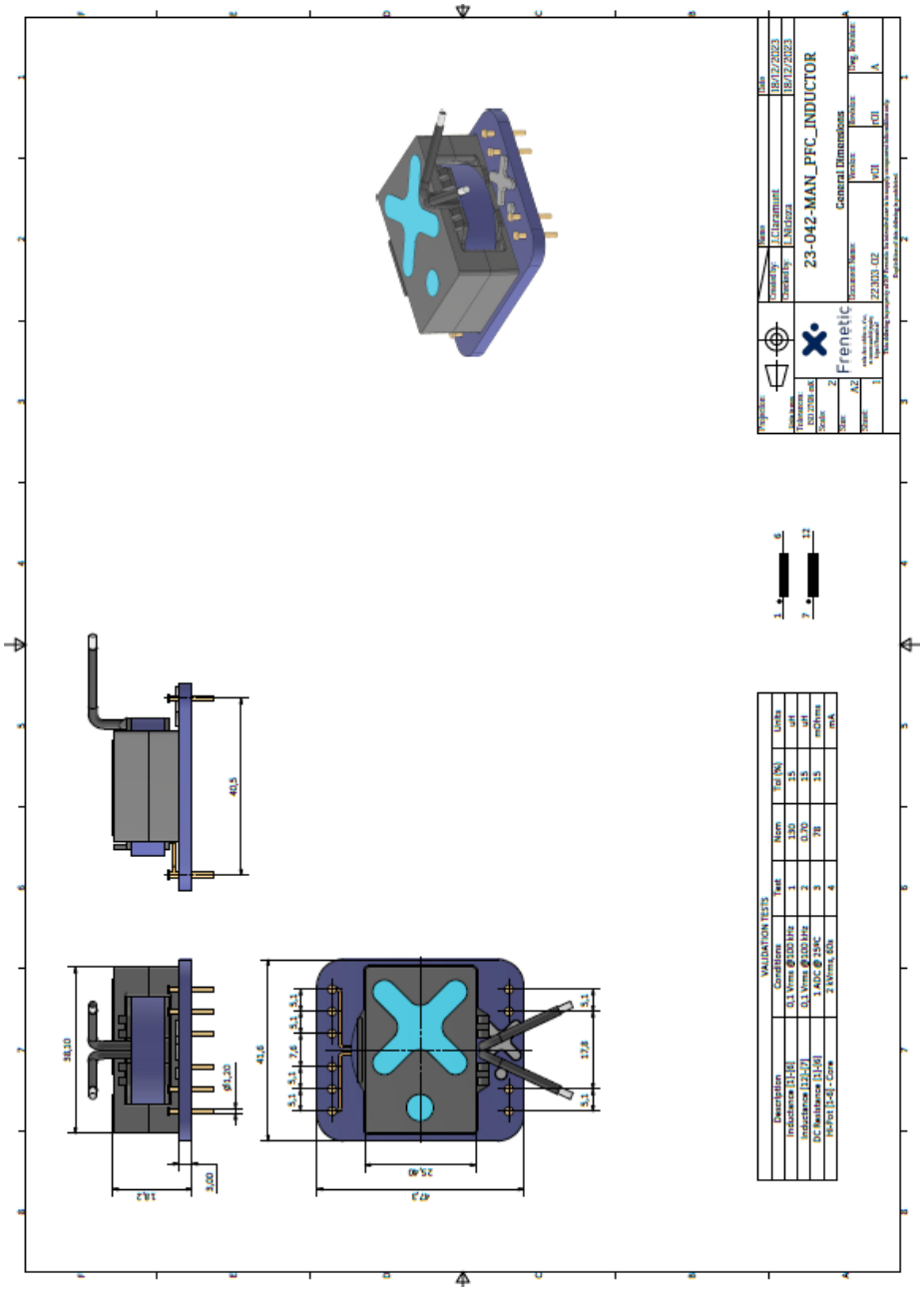


Figure 39 – Frenetic PFC inductor 22303-02-v01-r01 datasheet

12 Bill of Materials (BOM)

Table 7 – CGD 350W TPPFC EVB motherboard BOM

Designator	Fitted	Description	Manufacturer	Manu. P/N	Qty.
C6, C10	Y	CAP CER 1nF 50V 5% C0G/NP0 0603	Wurth Elektronik	885012006063	2
C2	Y	CAP CER 22pF 50V 5% C0G/NP0 0603	Wurth Elektronik	885012006053	1
C11, C14	Y	CAP CER 0.1uF 50V 10% X7R 0603	Wurth Elektronik	885012206095	2
C7	Y	CAP CER 10nF 50V 10% X7R 0603	Wurth Elektronik	885012206089	1
C24	Y	CAP POLY 0.82uF 560V 20% 18x11mm	Wurth Elektronik	890324025047CS	1
C26, C29	Y	CAP CER 1nF 630V 10% X7R 1206	Wurth Elektronik	885342208011	2
C19, C20	Y	CAP RAD 100uF 450V 20% 18X41.5mm	Wurth Elektronik	860241480001	2
C16	Y	CAP CER 0.1uF 50V 10% X7R 1206	Wurth Elektronik	885012208087	1
C15	Y	CAP CER 10uF 25V 10% X7R 1206	Wurth Elektronik	885012208069	1
C3	Y	CAP RAD 22uF 50V 20% 5x11mm	Wurth Elektronik	860020672011	1
C4	N	CAP CER 22nF 50V 10% X7R 0603	Wurth Elektronik	885012206091	1
C5	N	CAP CER 1uF 25V 10% X7R 0603	Wurth Elektronik	885012206076	1
C13	Y	CAP CER 22uF 25V 10% X5R 1206	Samsung	CL31A226KAHNNNE	1
C21, C22	Y	CAP CER 0.1uF 630V 10% X7R 1210	KEMET	C1210C104KBRACTU	2
C8, C9, C12	Y	CAP CER 220pF 50V 5% C0G/NP0 0603	Wurth Elektronik	885012006059	3
C27, C28	Y	CAP CER 2.2nF 500V 20% Y5U Radial 13x7mm	KEMET	C961U222MWWDBA7317	2
C23, C30	Y	CAP POLY 2.2nF 1.25kV 20% 13x4mm	KEMET	PHE850EA4220MA01R17	2
C1	Y	CAP CER 2.2nF 50V 20% X7R 0603	Wurth Elektronik	885012206085	1
C17, C18	N	CAP CER 0603			2
D7, D9	Y	Rectifier Diode, 3A, 1000V, DO-214AB	ON Semiconductor	S3M	2
D2, D8, D10	Y	Diode Schottky 30 V 200mA SOD-323	ON Semiconductor	BAT54HT1G	3
D6	Y	Diode Ultra Fast Rectifier 600V 1A SOD-123F	ON Semiconductor	ES1JFL	1
D5	Y	Diode Standard 100 V 200mA SOD-123	ON Semiconductor	MMSD4148T1G	1
D1, D3, D4	N	Diode Standard 100 V 200mA SOD-123	ON Semiconductor	MMSD4148T1G	3
J8, J9, J10, J11, J12	N	PC Pin Terminal Connector Through Hole 1.02mm diam.	Mill-Max	3103-2-00-15-00-00-08-0	5
J1	Y	CON 2WAY	Phoenix Contact	1984617	1
J2	N	CON 2WAY	Phoenix Contact	1984617	1
J3	Y	CON HDR 2WAY	Wurth Elektronik	61300421121	1
J7	Y	CON EDGE 26WAY	TE Connectivity	1761426-3	1
L2	Y	Inductor 150uH 5.4A	Wurth Elektronik	7447055	1
L1	Y	Line Common Mode Choke 7mH 7A	Wurth Elektronik	7448040707	1
M1, M2	Y	MOSFET N-CH 650V 44A TO-220	ON Semiconductor	FCPF067N65S3	2
Q1	N	Transistor NPN 40 V 200 mA SOT-23-3 (TO-236)	ON Semiconductor	MMBT3904LT1G	2
Q3	Y	Transistor NPN 40 V 200 mA SOT-23-3 (TO-236)	ON Semiconductor	MMBT3904LT1G	2
Q2	Y	Transistor PNP 40 V 200 mA SOT-23-3	ON Semiconductor	MMBT3906	1
R2, R3, R25	Y	RES SMD 10K 1% 1/8W 0603	Stackpole Electronics	RNCP0603FTD10K0	3
R1, R13, R4, R17	N	RES SMD 10K 1% 1/8W 0603	Stackpole Electronics	RNCP0603FTD10K0	4
R22, R23, R24, R26	Y	RES SMD 1K 1% 1/10W 0603	Yageo	RC0603FR-071KL	4
R42, R44	Y	RES SMD 0.25R 1% 2W 4527	Vishay Dale	WSR2R2500FEA	2
R19	N	RES SMD 0603			1
R35, R43	Y	RES SMD JUMPER 0R 0.05% 1/4W 1206	Panasonic	ERJ8GEY0R00V	2
R7, R8, R11, R12, R15, R16	Y	RES SMD 3.3M 1% 1/4W 1206	Vishay	CRCW12063M30FKEA	6
R20, R21, R27, R29, R31	Y	RES SMD 100K 1% 1/10W 0603	Stackpole Electronics	RMCF0603FT100K	5
R6	N	RES SMD NF 1206			1
R37, R41	Y	RES SMD 47K 5% 1/8W 0805	Vishay Dale	CRCW080547K0JNEA	2
R36, R40	Y	RES SMD 49.9R 1% 1/10W 0603	Yageo	AC0603FR-0749R9L	2
R28, R33, R39	Y	RES SMD 10R 1% 1/10W 0603	Yageo	RC0603FR-0710RL	3
R9, R10, R14	Y	RES SMD 2.49M 1% 1/4W 1206	Stackpole Electronics	RMCF1206FT2M49	3
R5	Y	RES SMD 1K 5% 1/2W 1206	Vishay Dale	CRCW12061K00JNEAHP	1
R30, R32	Y	RES SMD 4.99K 1% 1/10W 0603	Yageo	RC0603FR-074K99L	2
R18	Y	RES SMD 47.5K 1% 1/10W 0603	Stackpole Electronics	RMCF0603FT47K5	1
RT1	Y	THERM NTC 100K 5% 1/5W 0805	Murata	NCP21WF104J03RA	1
RT2	Y	Inrush Current Limiter 10R 3.7A 20% RAD15x7mm	TDK EPCOS	B57237S0100M000	1
RT3	Y	VARIS 400pF 4.5kA 517V RAD17x5.6mm	Littelfuse	V300LA20AP	1

Designator	Fitted	Description	Manufacturer	Manu. P/N	Qty.
S1	N	Tactile Switch SMD	Wurth Elektronik	435451019820	1
TP1, TP2, TP3, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP20, TP21, TP22, TP24, TP25, TP26, TP27, TP28	N	RED 1mm	Keystone Electronics	5000	25
TP4, TP19, TP23, TP29	N	BLACK 1mm	Keystone Electronics	5001	4
U1	Y	IC CRM PFC Controller SOIC-16	ON Semiconductor	NCP1680AAD1R2G	1
U2	Y	Half-Bridge Gate-Driver IC 8-SOIC	Texas Instruments	UCC27712DR	1
J4	Y	2 (1 x 2) Position Shunt Connector 10.16mm diam	Harwin	D3082-05	1
Z1	N	Zener Diode 4.7 V 500 mW SOD-123	ON Semiconductor	MMSZ5230BT1G	1
Z2	N	Zener Diode 15 V 500 mW SOD-123	ON Semiconductor	MMSZ4702T1G	1
Z3	y	Zener Diode 15 V 500 mW SOD-123	ON Semiconductor	MMSZ4702T1G	1
C25	Y	CAP POLY 3.3uF 275V 10% 31.5x16mm	Wurth Elektronik	890324027025CS	1
L4	Y	PFC Inductor	Wurth ElektronikFrenetic	750371793 22303-02-v01-r01	1
L3	Y	Common Mode Choke TH CHOKE 30mH 5A	Wurth Elektronik	7448050530	1
F1	Y	FUSE HOLDER	Wurth Elektronik	696108003002	1
	Y	Fuse	LittelFuse	0217005.MXP	
J5	Y	2 Position Terminal Block Header, Male Pins	Wurth Elektronik	691311500102	1
J6	Y	3 Position Terminal Block Header, Male Pins	Wurth Elektronik	691311500103	1
R34, R38	Y	RES THR 1.8K 5% 35W TO-220	Multicomp	MCTR35JDD1801	2
S2	Y	Pushbutton Switch	Multicomp	R13-24A-05-BB	1

Table 8 – Daughterboard BOM

Designator	Fitted	Description	Manufacturer	Manu. P/N	Qty.
D1	Y	Diode Ultra Fast Rec. 600V 1A 2-Pin SOD-123F	ON Semiconductor	ES1JFL	1
TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	N	Micro Pin	Keystone Electronics	1352-1	8
C2	Y	CAP CER 0.1uF 50V 10% X7R 0603	Wurth Elektronik	885012206095	1
C4	Y	CAP CER 0.1uF 50V 10% X7R 1206	Wurth Elektronik	885012208087	1
C3	Y	CAP CER 10uF 25V 10% X7R 1206	Wurth Elektronik	885012208069	1
C5, C6	N	CAP CER 0603			2
C1	Y	CAP CER 22uF 25V 10% X5R 1206	Samsung	CL31A226KAHNNNE	1
D2, D3, D4, D5	N	Diode Schottky 30 V 200mA SOD-323	ON Semiconductor	BAT54HT1G	4
R4, R6	Y	RES SMD 4.99K 1% 1/10W 0603	Yageo	RC0603FR-074K99L	2
TP1	N	Black PC Test Point, 1.02mm, Hole Diameter	Keystone Electronics	5001	1
C10, C11	Y	CAP CER 4.7uF 50V 10% X5R 0805	TDK	C2012X5R1H475K125AB	2
C9, C12	N	CAP CER 4.7uF 50V 10% X5R 0805	TDK	C2012X5R1H475K125AB	2
R1, R14, R16, R18, R20	Y	RES SMD JUMPER 0R 1/10W 0603	Stackpole Electronics	RMCF0603ZT0R00	5
R13, R15, R17, R19	N	RES SMD JUMPER 0R 1/10W 0603	Stackpole Electronics	RMCF0603ZT0R00	4
C7, C8	Y	CAP CER 0.1uF 630V 10% X7R 1210	KEMET	C1210C104KBRACTU	2
J7	N	CON MMCX-R-PC(40)	Wurth Elektronik	66012002111503	1
J8, J9	Y	CON MMCX-R-PC(40)	Wurth Elektronik	66012002111503	2
Q2, Q4	Y	ICeGaN 55mR DFN8x8	CGD	CGD65A055S2	2
Q1, Q3	N	ICeGaN 55mR DFN8x8	CGD	CGD65A055S2	2
R3, R7, R9, R11	N	RES SMD 2R 1% 1/16W 0603	TE Connectivity	CPF0603F2R0C1	4
R2	Y	RES SMD 10R 1% 1/10W 0603	Yageo	RC0603FR-0710RL	1
R10, R12	Y	RES SMD 10R 1% 1/10W 0603	Yageo	RC0603FR-0710RL	2
R5, R8,	N	RES SMD 10R 1% 1/10W 0603	Yageo	RC0603FR-0710RL	2
U1	Y	Half-Bridge Gate-Driver IC 8-SOIC	Texas Instruments	UCC27712DR	1

13 List of Figures

14 List of Tables

Dare to innovate differently

CAMBRIDGE GaN DEVICES

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